Allgemeines/Konstanten

$k = 8.617 \cdot 10^{-5} \frac{eV}{K} = 1.38 \cdot 10^{-23} \frac{J}{K}$
$e = 1.6022 \cdot 10^{-19} C$
$\varepsilon_0 = 8.854 \cdot 10^{-12} \frac{C}{Vm} = 8.854 \cdot 10^{-14} \frac{C}{Vcm}$
$\varepsilon_r(\text{Si}) = 11.8 \quad \varepsilon_r(\text{SiO}_2) = 3.9 \approx 4$

Temperaturspg.: $V_{\text{th}} = \frac{kT}{q} \overset{T=300K}{\approx} 26mV$

$n_i = 1.45 \cdot \frac{10^{10}}{cm^3}$
$1\mathring{A} = 10^{-10}m = 10^{-8}cm$
$C_{\text{g}} = 2\frac{fF}{\mu m} \quad C_{\text{eff}} = 1\frac{fF}{\mu m} \quad C_{\text{OL}} = 0.25\frac{fF}{\mu m}$
Si: $E_c - E_v = 1.1eV$

c	m	μ	n	p	f
10^{-2}	10^{-3}	10^{-6}	10^{-9}	10^{-12}	10^{-15}

Frequenz: $f = \frac{1}{T}$

Bool'sche Logik

De-Morgan: $\overline{a \wedge b} = \overline{a} \vee \overline{b} \quad \overline{a \vee b} = \overline{a} \wedge \overline{b}$
Absorption: $a \vee (a \wedge b) = a \quad a \wedge (a \vee b) = a$
Konsensus
$(a \vee b)(\overline{a} \vee c)(b \vee c) = (a \vee b)(\overline{a} \vee c)$
$ab \vee \overline{a}c \vee bc = ab \vee \overline{a}c$

Kondensator

Aufladung

$V_{\text{out}} = V_{\text{in}} \cdot \left(1 - e^{\frac{-t}{\tau}}\right)$
$t = -\tau \cdot \ln\left(1 - \frac{V_{\text{out}}}{V_{\text{in}}}\right)$

Entladung

$V_{\text{out}} = V_{\text{in}} \cdot \left(e^{\frac{-t}{\tau}}\right)$
$t = -\tau \cdot \ln\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right)$
$\tau = RC$

Ladung des Kondensators

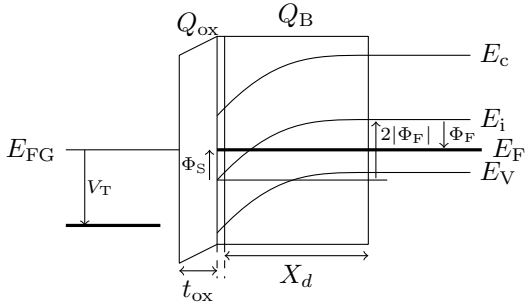
$Q = CV$

Strom des Kondensators

$I = \frac{dQ}{dt}$

MOS Transistor

Intrin. Ladungsträger-Konzentration
$n_i = 1.45 \cdot 10^{10} cm^{-3}$
Mass-Action-Law: $np = n_i^2$
Im n-dotierten Halbleiter:
$n \approx N_D \gg n_i \qquad p = \frac{n_i^2}{N_D}$
Im p-dotierten Halbleiter:
$p \approx N_A \gg n_i \qquad n = \frac{n_i^2}{N_A}$



Effektives Fermi-Niveau:
$q\phi_{\text{F}} = E_F - E_{Fi}$
NMOS: $\phi_{\text{F}_p} = \frac{kT}{q} \ln\left(\frac{n_i}{p}\right) (< 0)$
PMOS: $\phi_{\text{F}_n} = \frac{kT}{q} \ln\left(\frac{n}{n_i}\right) (> 0)$
Oxid-Kapazität:
$C_{\text{ox}} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad \varepsilon_{ox} = \varepsilon_r \cdot \varepsilon_0$
Oxid-Dicke:
$t_{ox} \leq 5nm \overset{\mathring{A}=10^{-10}m}{=} 50\mathring{A}$
Weite der Raumladungszone:
$X_d = \sqrt{\frac{2\varepsilon_{Si}|\phi_S - \phi_F|}{qN_A}}$
Maximum bei $\phi_S = -\phi_F$
Ladung der Raumladungszone:
$Q_B = \pm qNX_d = \pm\sqrt{2qN_A\varepsilon_{Si}|\phi_S - \phi_F|}$ $\left[\frac{C}{cm^2}\right]$
Maximum bei $\phi_S = -\phi_F$
(-: NMOS, +: PMOS)

Potentialdifferenz Gate-Substrat:

$\phi_{GC} = \phi_G - \phi_C$
Flatband Voltage: $V_{\text{FB}} = \phi_{GC} - \frac{Q_{ox}}{C_{\text{ox}}}$
Threshold Voltage
$V_{\text{T}} = V_{\text{T0}} + \gamma\left(\sqrt{V_{\text{SB}} + 2|\phi_F|} - \sqrt{2|\phi_F|}\right)$
$V_{\text{T0}} = V_{\text{FB}} - 2\phi_F - \frac{Q_B}{C_{\text{ox}}}$
Verschieben von V_{T}
$N_I = \frac{Q_I}{q} = \frac{C_{\text{ox}}\Delta V}{q}$

Velocity-Saturated Current Equations

Effektive Mobilität
$\mu_e = \frac{\mu_0}{1 + \left(\frac{V_{\text{GS}} - V_{\text{T}}}{\Theta \cdot t_{ox}}\right)^{\eta}}$
Body-Factor
$\gamma = \frac{1}{C_{\text{ox}}}\sqrt{2q\varepsilon_{si}N_A}$ $[V^{0.5}]$
Querstrom (eingeschwungen)
$I_{\text{DC}} = \frac{V_{\text{DD}} - V_{\text{oL}}}{R_{\text{L}}}$
$E_{cn} = 6 \cdot 10^4 \frac{V}{cm}$
$E_{cp} = 24 \cdot 10^4 \frac{V}{cm}$
$V_{\text{Dsat}} = \frac{(V_{\text{GS}} - V_{\text{T}}) \cdot E_c L}{(V_{\text{GS}} - V_{\text{T}}) + E_c L}$

Transconductance Parameter
$k' = \mu_n C_{\text{ox}} \qquad k = k'\frac{W}{L}$

Alpha-Power Law:

$I_{\text{DS}} = K_S \frac{W}{L}(V_{\text{GS}} - V_{\text{T}})^{\alpha}$ mit $\alpha \approx 1.25$
$I_{\text{DS}} = K_L \frac{W}{L}(V_{\text{GS}} - V_{\text{T}})V_{\text{DS}}$
$\Rightarrow V_{\text{Dsat}} = \frac{K_S}{K_L}(V_{\text{GS}} - V_{\text{T}})^{\alpha - 1}$

Bereichs-Abschätzung:

$V_{\text{GS}} < V_{\text{T}} \rightarrow$ sicher Cutoff
$V_{\text{DS}} > V_{\text{GS}} \rightarrow$ wahrsch. Sättigung
$V_{\text{DS}} < V_{\text{GS}} \rightarrow$ wahrsch. linearer Bereich
$V_{\text{DS}} = V_{\text{GS}} \rightarrow$ sicher Sättigung

I_{D} long channel

$V_{\text{DS}} < V_{\text{GS}} - V_{\text{T}}$: linear
$I_{\text{D}} = \frac{k}{2}\left[(V_{\text{GS}} - V_{\text{T}})V_{\text{DS}} - V_{\text{DS}}^2\right]$
$V_{\text{DS}} \geq V_{\text{GS}} - V_{\text{T}}$: saturation
$I_{\text{D}} = \frac{k}{2}(V_{\text{GS}} - V_{\text{T}})^2(1 + \lambda V_{\text{DS}})$

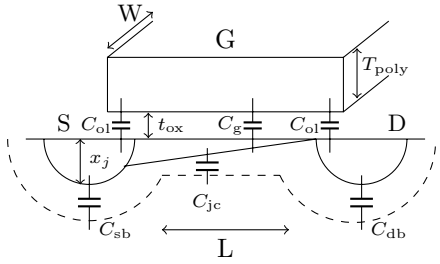
I_{D} short channel (!)

$V_{\text{DS}} \geq \frac{(V_{\text{GS}} - V_{\text{T}})E_c L}{(V_{\text{GS}} - V_{\text{T}}) + E_c L}$: linear:
$I_{\text{DS}} = \frac{W}{L}\frac{\mu_e C_{\text{ox}}}{\left(1 + \frac{V_{\text{DS}}}{E_c L}\right)}\left(V_{\text{GS}} - V_{\text{T}} - \frac{V_{\text{DS}}}{2}\right)V_{\text{DS}}$
$V_{\text{DS}} < \frac{(V_{\text{GS}} - V_{\text{T}})E_c L}{(V_{\text{GS}} - V_{\text{T}}) + E_c L}$: saturation
$I_{\text{DS}} = WC_{\text{ox}}\frac{(V_{\text{GS}} - V_{\text{T}})^2 v_{sat}}{V_{\text{GS}} - V_{\text{T}} + E_c L}$ mit $v_{sat} = \frac{E_c \mu_e}{2}$

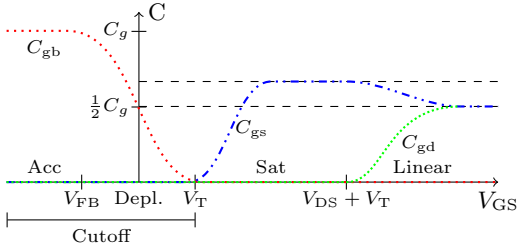
Diode

$I_{\text{D}} = I_{\text{S}}\left(\exp(V_{\text{J}}/V_{\text{th}}) - 1\right)$
$\phi_B = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$
$C_{\text{j0}} = \frac{\varepsilon_{Si}}{X_d} = \sqrt{\frac{\varepsilon_{Si}q}{2\phi_B} \cdot \frac{N_A N_D}{N_A + N_D}}$ $\left[\frac{fF}{\mu m^2}\right]$
Beim abrupten pn Übergang:
$C_{\text{j0}} \approx \sqrt{\frac{\varepsilon_{Si}qN_A}{2\phi_B}}$

MOS Capacitances



Thin-Oxide (→ Gate) Capacitance
$C_{\text{G}} = WC_{\text{g}}$
$C_{\text{g}} = LC_{\text{ox}} = L\frac{\varepsilon_{ox}}{t_{ox}} = 1.6\frac{fF}{\mu m}$
Bereiche



	C_{GS}	C_{GD}	C_{GB}
Cutoff ($V_{\text{GS}} = 0$)	0	0	$\frac{1}{2}C_{\text{g}}$
Linear	$\frac{1}{2}C_{\text{g}}$	$\frac{1}{2}C_{\text{g}}$	0
Sättigung	$\frac{2}{3}C_{\text{g}}$	0	0

pn Junction Capacitance:

Bottom Area: $A_b = WY$
Sidewall Area: $A_{sw} = Wx_j$
$C_{\text{J}} = \frac{C_{\text{jb}}(A_b + A_{sw})}{\left(1 - \frac{V_{\text{J}}}{\phi_B}\right)^m} = \frac{C_{\text{jb}}W(Y + x_j)}{\left(1 - \frac{V_{\text{J}}}{\phi_B}\right)^m}$
abrupter Übergang: $m = 0.5$
$K_{eq} = \frac{C_{eq}}{C_{jb}} = \frac{-2\phi_B^{\frac{1}{2}}}{V_2 - V_1}\left[(\phi_B - V_2)^{\frac{1}{2}} - (\phi_B - V_1)^{\frac{1}{2}}\right]$
Large Signal effective C_{J}:
$C_{\text{J}} = K_{eq}C_{\text{jb}}W(Y + x_j) = C_{\text{j}}W$

Overlap Capacitance:

$C_{\text{ol}} = C_{ov} + C_f$
$C_{\text{f}} = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1 + \frac{T_{\text{poly}}}{t_{\text{ox}}}\right)$
$C_{\text{ov}} = C_{\text{ox}} \cdot L_D$

Noise Margin

Single Source (SSNM):

$\text{SSNM}_H = V_{\text{oH}} - V_{\text{S}}$
$\text{SSNM}_L = V_{\text{S}} - V_{\text{oL}}$

Multiple Source (MSNM):

$\text{NM}_H = V_{\text{oH}} - V_{\text{iH}}$
$\text{NM}_L = V_{\text{iL}} - V_{\text{oL}}$

MOS Inverter

Resistive-Load-Inverter

$V_{\text{oL}} \approx \frac{V_{\text{DD}}}{1 + kR_{\text{L}}(V_{\text{DD}} - V_{\text{T}})}$
$V_{\text{oH}} = V_{\text{DD}}$
$V_{\text{iL}} = V_{\text{T}} + \frac{1}{kR_{\text{L}}}$
$V_{\text{iH}} = V_{\text{T}} + \sqrt{\frac{8V_{\text{DD}}}{3kR_{\text{L}}}} - \frac{1}{kR_{\text{L}}}$
$V_{\text{S}}: \frac{Wv_{sat}C_{ox}(V_{\text{S}} - V_{\text{T}})^2}{(V_{\text{S}} - V_{\text{T}}) + E_c L} = \frac{V_{\text{DD}} - V_{\text{S}}}{R_{\text{L}}}$

$V_S = -\frac{\frac{V_T^2 R_L k E_c L}{2} + V_{DD}V_T - V_{DD}E_cL}{V_T R_L k E_c L + V_{DD} + V_T - E_c L}$

$V_{ouL} = \sqrt{\frac{2V_{DD}}{3kR_L}}$

$V_{ouH} = ?$

$I_{DSmax} = \frac{V_{DS}-V_{oL}}{R_L}$ wenn $V_{out} = V_{oL}$

Saturated Enhancement Load

$V_{SB} = V_{oH} = V_{DD} - V_T$

$V_{oH} = V_{DD} - V_T(V_{oH})$

(iter. Lösungsverfahren mit $V_{OH,start} = V_{DD} - V_T$)

$\frac{W_I}{L_I}\frac{\mu_n C_{ox}}{1+\frac{V_{out}}{E_{CN}L_I}}\left[(V_{in}-V_{TI})V_{out} - \frac{V_{out}^2}{2}\right] = \frac{W_L V_{sat} C_{ox}(V_{DD}-V_{out}-V_{TL})^2}{(V_{DD}-V_{out}-V_{TL})+E_{CN}L_L}$

CMOS Inverter

$V_{oH} = V_{DD} \qquad V_{oL} = 0V$

$V_{iL} = \frac{2V_{out}-V_{DD}-|V_{TP}|+(k_N/k_P)V_{TN}}{1+(k_N/k_P)}$ mit $V_{out} = V_{ouL}$

$V_{iH} = \frac{2V_{out}+V_{TN}+(k_N/k_P)(V_{DD}-|V_{TP}|)}{1+(k_N/k_P)}$ mit $V_{out} = V_{ouH}$

$\chi = \sqrt{\frac{\frac{W_N}{E_{CN}L_N}}{\frac{W_P}{E_{CP}L_P}}} = \sqrt{\frac{W_N\mu_n}{W_P\mu_p}}$

$V_S = \frac{V_{DD}-|V_{TP}|+\chi V_{TN}}{1+\chi}$

Pseudo-NMOS Inverter

$V_{oH} = V_{DD}$

$V_{oL}: I_{DP}(\text{sat}) = I_{DN}(\text{lin})$

$\frac{W_P v_{sat} C_{ox}(V_{DD}-|V_{TP}|)^2}{V_{DD}-|V_{TP}|+E_{cp}L_P} = \frac{W_N}{L_N}\frac{\mu_N C_{ox}}{\left(1+\frac{V_{oL}}{E_{CN}L_N}\right)}\left((V_{DD}-V_{TN})V_{oL} - \frac{V_{oL}^2}{2}\right)$

Inverter Sizing

50% Point: $t_{phl} = t_{plh} = 0.69R_{eff}C_L$

Equivalent On-Resistances

$R_{eqn} = 12.5\frac{k\Omega}{\square} \qquad R_{eqp} = 30\frac{k\Omega}{\square}$

Pull-Down / Pull-Up Resistance

$R_N = R_{eqn}\cdot\frac{L_N}{W_N} \qquad R_P = R_{eqp}\cdot\frac{L_P}{W_P}$

$R_N = \frac{V}{0.7I_{Dsat,n}} \qquad R_P = \frac{V}{0.7I_{Dsat,p}}$

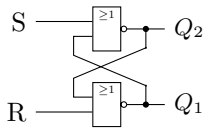
Series Stack: $W_{eq} = \frac{W_1W_2W_3}{W_1W_2+W_2W_3+W_1W_3}$

Parallel Devices: $W_{eq} = W_1 + W_2 + W_3$

Latches und FFs

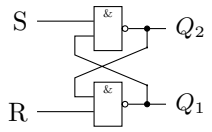
RS Latch NOR, active high

	S	R	Q_1	Q_2
hold	0	0	$\overline{Q_2}$	$\overline{Q_1}$
reset	0	1	0	1
set	1	0	1	0
	1	1	0	0



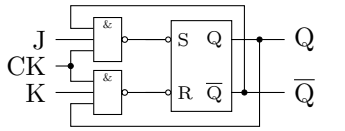
RS Latch NAND, active low

	S	R	Q_1	Q_2
	0	0	1	1
set	0	1	1	0
reset	1	0	0	1
hold	1	1	$\overline{Q_2}$	$\overline{Q_1}$

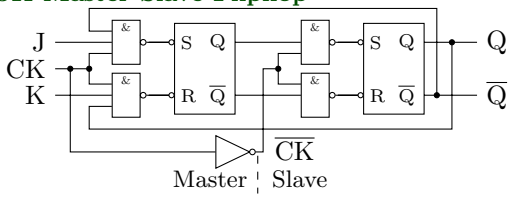


JK Flipflop, active high

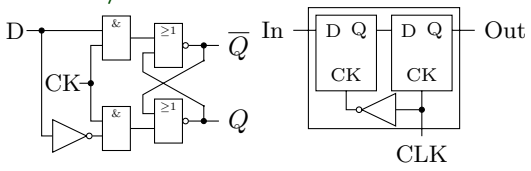
J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$



JK Master-Slave Flipflop



D Latch / FF



CMOS Power Dissipation

Static (Standby) Power

$P_{DC} = I_{DC}V_{DD}$

$P = \alpha C V_{DD}^2 f_{CLK} + I_{leak}V_{DD}$

Dynamic (Switching) Power

Capacitance Switching Current / Power

$I_{D,avg} = C\frac{dV}{dt} = \frac{C_L\Delta V_{swing}}{\Delta t} = C_L V_{DD} f_{avg}$

$P_{cap} = I_{D,avg}V_{DD} = C_L V_{DD}^2 f_{avg} = \alpha_{0\to1} C_L V_{DD}^2 f_{clk}$

$\alpha_{0\to1} = \frac{\#\text{toggles}}{2\#\text{clock cycles}}$

Crowbar Current / Power

$I_{SC} = \frac{\Delta t_{sc}}{T} I_{SC,avg}$ mit $\Delta t_{sc} = \Delta t_{scr} + \Delta t_{scf}$

$P_{SC} = \Delta t_{SC} I_{SC,avg} V_{DD} f_{clk} = C_{SC} V_{DD}^2 f_{clk} = \alpha_{SC} C_L V_{DD}^2 f_{clk}$

$P_{switching} = P_{cap} + P_{SC} \overset{\alpha=\alpha_{0\to1}+\alpha_{SC}}{=} \alpha C_L V_{DD}^2 f_{clk}$

Power and Delay Tradeoffs

$PDP = Pt_p = \frac{1}{2}CV_{DD}^2$

$EDP = PDP \cdot t_p = \frac{C^2 V_{DD}^3}{2K_2(V_{DD}-V_T)}$ $[Js]$

$t_p = \frac{1}{2f}$

Wire Capacitance

$C_{wire} = C_{int}L_W = 0.2\frac{fF}{\mu m}\cdot$ wire length

$C_{load} = C_{fanout} + C_{self} + C_{wire}$

Path Delay Optimization

total_delay $\approx \sum_i R_i C_i$

Fanout Ratio: $f = \frac{C_{out}}{C_{in}}$

$\gamma_{inv} = \frac{C_{self}}{C_{in}}$

$\tau = R_{eff}C_{in}$ $\qquad \tau_{inv} = 3R_{eqn}C_g L_n$

$\tau_{nand} = 4R_{eqn}C_g L_n \qquad \tau_{nor} = 5R_{eqn}C_g L_n$

$t_{delay} = R_{eff}(C_{out}+C_{self}) = \tau_{inv}\left(\frac{C_{out}}{C_{in}} + \gamma_{inv}\right)$

$t_p = \frac{t_{phl}+t_{plh}}{2}$

$t_{Elmore} = R_1C_1 + (R_1+R_2)C_2$

total_delay $= \sum_{j=1}^{N}\tau\left(\frac{C_{j+1}}{C_j}+\gamma\right) = \sum_{j=1}^{N}\tau\left(\frac{W_{j+1}}{W_j}+\gamma\right)$

$W_j = \sqrt{W_{j-1}W_{j+1}}$

fanout_delay $= \tau\frac{C_{j+1}}{C_j}$

optimal_fanout_delay $= (\prod \text{fanout\_delay})^{\frac{1}{N}}$

$f^N C_{in} = C_{load}$

Logical Effort

$LE = \frac{\tau_{gate}}{\tau_{inv}} = \frac{(R_{eff}C_{load}C_{in})_{gate}}{(R_{eff}C_{load}C_{in})_{inv}}$

$LE_{inv} = 1 \quad LE_{nand} = \frac{4}{3} \quad LE_{nor} = \frac{5}{3}$

Parasitic Term: $P = LE\cdot\gamma$

Normalized delay

$D = \frac{\text{total\_delay}}{\tau_{inv}} = \sum(LE\cdot FO + P) = N\cdot SE^* + \sum P$

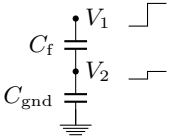
Fanout: $FO = \frac{C_{j+1}}{C_j}$

total_path_effort $= \prod(LE\cdot BE\cdot FO) = \prod LE\cdot BE\frac{C_{load}}{C_{in}}$

optimal_stage_effort: $SE^* = \text{total\_path\_effort}^{\frac{1}{N}}$

Capacitive Feedthrough

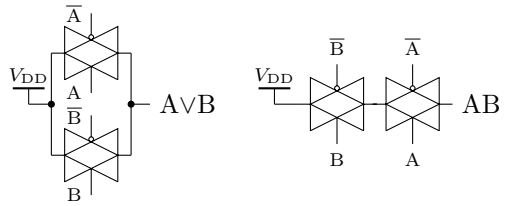
$\Delta V_2 = \frac{C_f}{C_f+C_{gnd}}\Delta V_1$



Charge Sharing

$V^* = \frac{C_1V_1+C_2V_2}{C_1+C_2}$

CMOS Transmission Gate

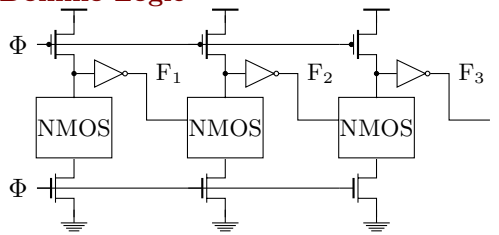


$R_{TG} = R_{eqn}\frac{L}{W}$

$C_{in,off} = C_{out,off} = C_{eff}(W_N + W_P) = C_{eff}2W$

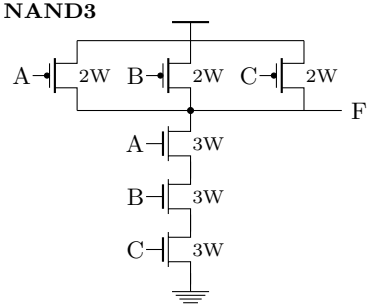
$C_{in,on} = C_{out,on} = C_{eff}2W + C_gW$

Domino Logic



Logical Effort

NAND3



NOR3