Mitschrift
Entwurf integrierter Schaltungen
Wintersemester 2013/14

17. Februar 2014

Inhaltsverzeichnis

1 Introduction

- addresses the design of digital circuits
- train you to think like a circuit designer
- achive a good balance among `speed, power consumption, reliability`
- digital integrated circuit design in 0.18 μm and 0.13 μm

Contributions from several engineering specialists:

- system designer
- register transfer level (RTL) language
- logic design (gate level)
- circuit level (transistor schematic)
- geometric layout level (GDS-II)

3 Dinge für funktionierende Schaltung nötig:

- based on integrated circuit technology
  - circuit families
  - level of integration
  - programmable vs. fixed function

MOS/CMOS

- focus on circuit simulation
- hand analysis

Major DSM device and interconnect issues

DSM Devices

- short-channel-effects on V_T (Threshold Voltage)
- velocity saturation
- thin-oxide (tunneling / breakdown)
- subthreshold current
- DIBL (`device induced barrier lowering`)
- Hot-carrier effect (Elektronenbewegung durch Hitzeeffekte)
- thin-oxide gate leakage (Leckströme Gate-Substrat)
- RC delay (Parasitäre Widerstände [?])
- IR drop (dünnere Leitungen → Widerstand → Spannungsabfall auf Versorgungsleitungen → Spannung an Bauteil fehlt)
- L di/dt (schnellere Bauteille → höhere Frequenzen möglich, dadurch aber Nebeneffekte)

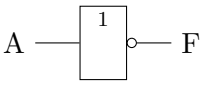
- capacitive coupling (dünne, nahe beieinander liegende Leitungen → aufgestellte Platten → Kapazität zwischen Leitungen)
- inductive coupling (Leitungen sind in Relation zum Bauteil lang)
- electromigration (hoher Stromfluss → Material wird in eine bestimmte Richtung abgetragen → Leitungen werden abgetragen)
- antenna effects (Schleife wird zur Antenne: muss verhindert werden)
- Clock Skew (Verschiedene Gates erhalten das Clock Signal zu unterschiedlichen Zeitpunkten aufgrund von (tlw. obigen) Effekten an den Leitungsbahnen)

2 Review of Digital Logic Gate Design

Wahrheitstabelle: Wurde als „Was wäre wenn"-Tabelle bezeichnet:
Die Großbuchstaben A, B und F beschreiben die Verdrahtung, tatsächlich werden sie in diesem Kontext aber als Stellvertreter für das Signal benutzt.

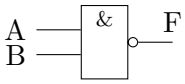
2.1 Basic Logic Funtions: `INV`, `NAND`, `NOR`

INV



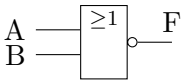
A	F
0	1
1	0

NAND



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

NOR

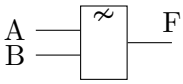


A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

2.2 Combinational Logic

- sum-of-products (DNF): $F = AC \vee BC \vee AD \vee BD$
- product-of-sums (KNF): $F = (A \vee B)(C \vee D)$

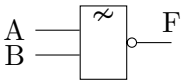
XOR



A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

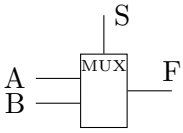
$F = A \oplus B = A\overline{B} \vee \overline{A}B$

XNOR



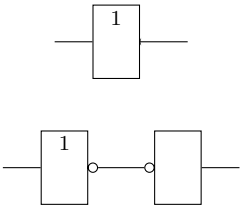
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

MUX



$F = AS \vee B\overline{S}$

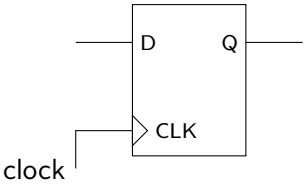
Buffer / Refresher



Erneutes Erzeugen der Information durch Batteriespannung, kein direktes Durchschalten des Eingangssignals.

2.3 Sequential Logic Elements

FlipFlop (FF)	not transparent (logisch!)
Latch	transparent



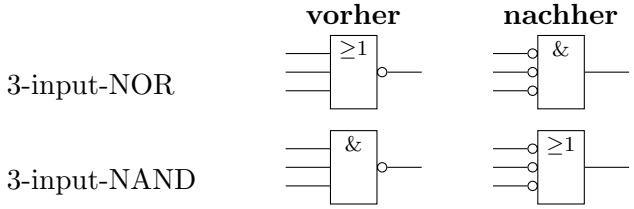
$\mathbf{Q}^a$	C	D	$\mathbf{Q}^n$
0	0	-	0
1	0	-	1
-	$0 \to 1$	0	0
-	$0 \to 1$	1	1
0	1	-	0
1	1	-	1
0	$1 \to 0$	-	0
1	$1 \to 0$	-	1

Excitation Table
(Schaltfolgetabelle)
„-“heisst „Don’t Care“.

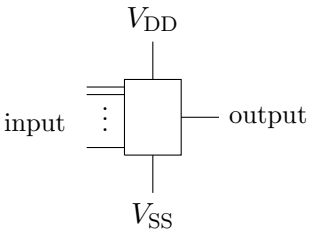
C	D	$\mathbf{Q}^n$
0	-	Q^a
1	-	Q^a
$0 \to 1$	0	0
$0 \to 1$	1	1
$1 \to 0$	-	Q^a

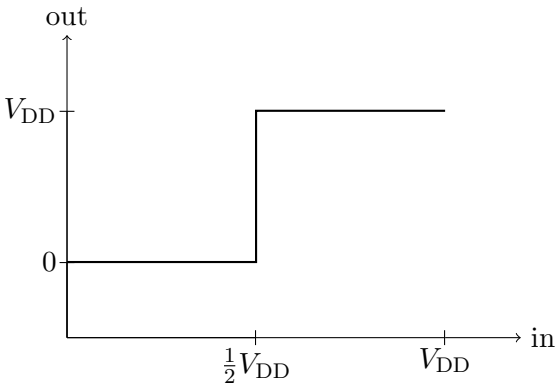
Zusammengefasst zur
Reduced Excitation Table

Anmerkung zu De Morgan
De Morgan sollte nicht auf Schaltungen angewendet werden, da diese unverständlich werden:



2.4 Implementation of Logic Circuits

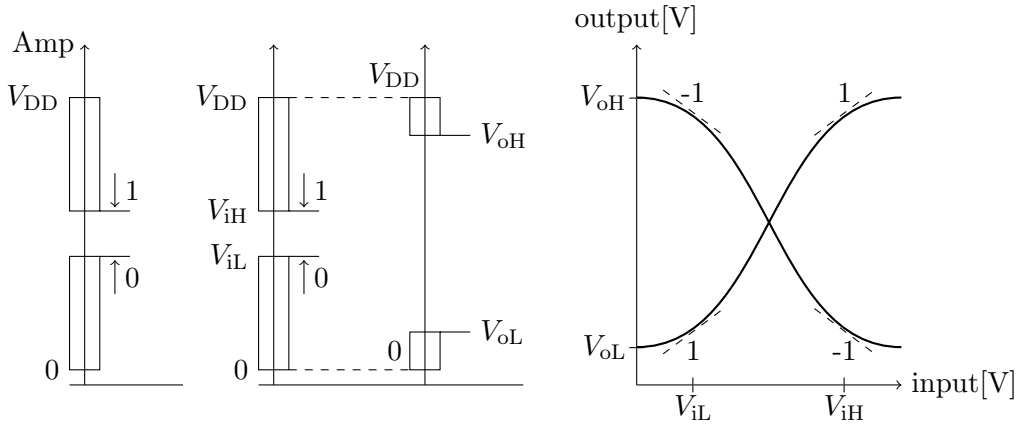




2 logic levels: 0 and 1

- Input impedance $\rightarrow \infty$
  High Input Impedance $\rightarrow$ Little Loading on Driving Signal
- Output impedance $\rightarrow 0$
  Low Output Impedance $\rightarrow$ Large Currents $\rightarrow$ stable Output Voltage
- Power Consumption ≈ 0
- No Time Delay (Latency)

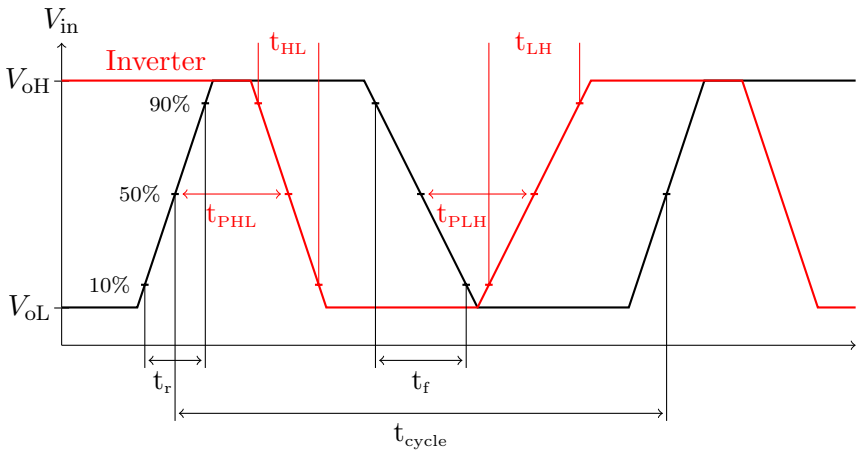
Logic abstraction of continous singals:



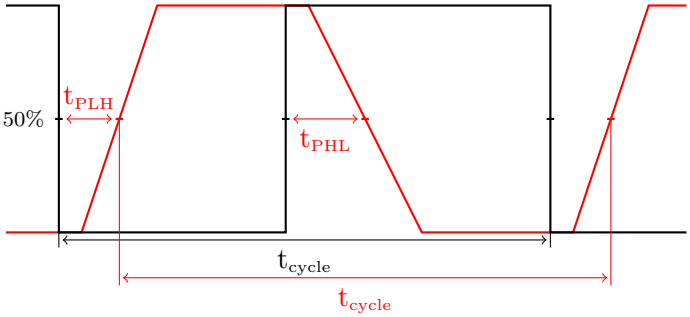
(the input voltages V_{iL} and V_{iH} are defined by the points at which the magnitude of the slope of the voltage transfer characteristic is 1)

- functional (Schaltung muss eine binäre Funktion darstellen)
- Quantisation (Überführung von kontinuierlichen in diskrete Werte)
  $\geq V_{\mathrm{iH}} \rightarrow$ logical 1
  $\leq V_{\mathrm{iL}} \rightarrow$ logical 0
- Regeneration (Refreshen der Spannungslevels für logische 0 (V_{SS}) und 1 (V_{DD}))
- Directivity (Changes in an output level should not appear at any input of the same circuit)
- Fanout / Fanin (Anzahl der Schaltungen, die an die Ausgänge bzw. die Eingänge gehängt werden können)
- Noise Margin:
  $\mathrm{NM}_H = V_{\mathrm{oH}} - V_{\mathrm{iH}}$
  $\mathrm{NM}_L = V_{\mathrm{iL}} - V_{\mathrm{oL}}$
  The circuit is working properly if Noise is inside these ranges
- „Output Signal should be better than Input Signal“

- Definition of Transient Characteristics
  (Schwarz: Input Voltage over Time, Rot: Output Voltage over Time)



Für Berechnungen von Hand → Oftmals Verwendung von idealen Eingangssignalen (Steigung ∞)
t_r: rise time, t_f: fall time, t_{HL}: time high-low, t_{LH}: time low-high
t_{PHL}: time propagation high-low, t_{PLH}: time propagation low-high



- finite rise and fall delays
- finite propagation times
- critical path (Wahl des schlechtesten Pfad, Verbesserung dessen Delays um Spezifikation zu erfüllen)
- glitches (kurzzeitiges, instabiles Ausgangssignal aufgrund verschiedener Laufzeiten unterschiedlicher Signalpfade in einer Schaltung)
- cycle time = $\frac{1}{\text{clock frequency}}$
  Das Eingangssignal darf nicht schneller sein als das Propagation Delay
  →clock= 20..50·propagation delay für gut funktionierende Bauteile

2.5 Power Estimation

- gate switching consumes power
- minimization per logic operation
  varies for
  - logic (intern asynchron, output mit clock; wird hochgefahren bei Bedarf)

  - memory (je nach Gebrauch; eher selten)
  - clock (arbeitet immer)
  - analog blocks (je nach Gebrauch)
- $P = I \cdot V_{\text{DD}}$
  where I is the current flowing from V_{DD} to Gnd
- static and dynamic power
  $P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}}$
- $P_{\text{static}} = (I_{DC} + I_{\text{leakage}}) \cdot V_{\text{DD}}$
  Verbrauch, wenn das Gate nicht switcht
- $P_{\text{dynamic}} = C \cdot V_{\text{DD}}^2 \cdot f \qquad (\uparrow \text{f} \rightarrow \uparrow \text{C})$
  Verbrauch, wenn das Gate switcht
  Treiberfähigkeit C $\Rightarrow$ balance of power and delay
- Höhere Frequenz verbraucht mehr Leistung

2.6 Digital Integrated Circuit Design

Simply stated, design is the effective management of a large number of engineering tradeoffs.

- timing ↑ (Anforderungen an Geschwindigkeit steigen)
- power ↑ (Immer mehr Gatter auf einer Fläche)
- area ↓ (Immer kleinere Strukturen)
- reliability ↑ (Anforderung an Lebensdauer [z.B. Flugzeug] steigen)
- and others
  - noise tolerance
  - testability
  - yield
  - temperature
  - supply fluctuations
  - time-to-market
  - cost
  - packaging

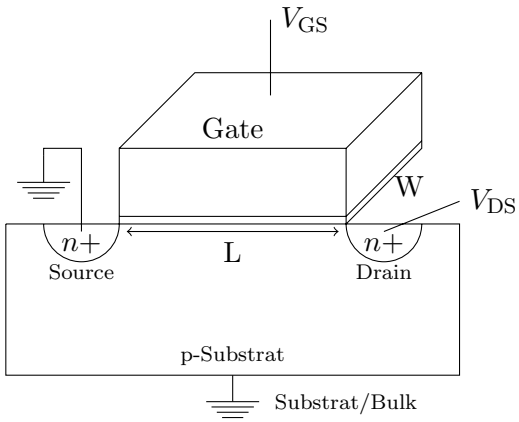
A popular missconception is that good circuit design includes new and innovative circuit topologies. Instead:

- first time right
- low cost
- time to volume (Zeit zur Massenfertigung)
- properly working for the expected lifetime

2.7 MOS Transistor Structure and Operation

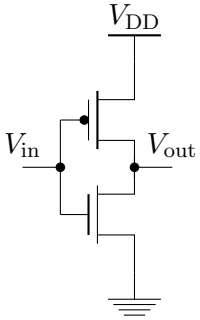
- behaves like a switch
- can be used to build up complex logic functions:
  `INV, BUFFER, NOR, NAND, MUX, D-FF`

NMOS



- poly silicon
- isolator (silicondioxide)
- threshold voltage V_{Th}

Complementary MOS (CMOS)



PMOS (pull up)

NMOS (pull down)

V_{in}	0	1
PU	1	*
PMOS	leitet	sperrt
PD	*	0
NMOS	sperrt	leitet
V_{out}	$1 \vee * = 1$	$0 \vee * = 0$

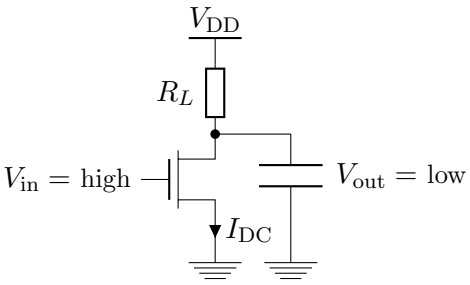
* = undefined / hochohmig

Stromfluss nur beim Umschalten → weniger Leistungsverbrauch

Steady-State-Power

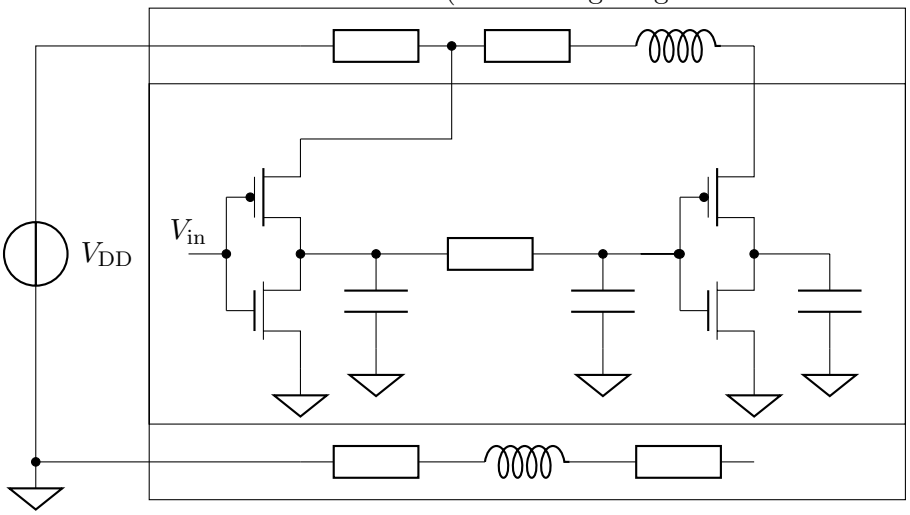
$$I_{DC} = \frac{V_{DD} - V_{oL}}{R_L}$$

⇒ CMOS exhibits low standby power



2.8 Deep Submicron (DSM) Interconnect

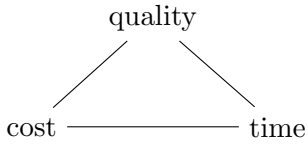
- to provide interconnects between gates
- to route the power supply and ground to all gates
- capacitance to ground
- interconnect issues now dominate the
  - performance ($\rightarrow$ Timing)
  - reliability ($\rightarrow$ Electromigration)
  - power distribution
- Possible Solution: Buffer insertion (um Leitungslänge in Griff zu bekommen)



2.9 Computer-Aided-Design (CAD) of Digital Circuits

- essential to the design process today
  - front-end, back-end tools
    - high-level description to gate-level design
    - physical design (Gate-Level Design to geometric layout in GDS-II)
  - ASIC vs. Full Custom
    - repetitive structures (data path, memory)
- SPICE (Netzwerktheorie)
  - nonlinear DC
  - large signal time domain (transient)
  - small-signal frequency domain
  - 1st MUST: mathematical / numerical model
  - 2nd MUST: apply practical parameters

- magic triangle



- most important design spec today:
  - time-to-market
  - time-to-volume
- Increasingly important specs in Europe (to differentiate from competition): Safe, Secure (Datensicherheit) & Reliable Circuits (SSRC)
  The Callenges Ahead
  - Understanding
  - Knowledge
  - Creativity
  - Reuse in other disciplines

3 MOS Transistor

- metal-oxide-semiconductor field-effect transistor
- MOS devices (Übergang Metall → Oxid), pn junctions, device capacitances
  - threshold voltage
  - current equations
  - capacitance models
- enhancement-mode devices (turn on voltage > 0V, Anreicherung)
- depletion-mode devices (turn on voltage > V_T, Verarmung)

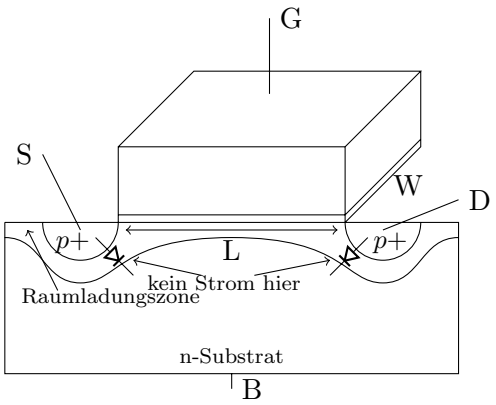
Zuerst: back_of_the_envelope or hand calculations („um kreativ zu werden“)

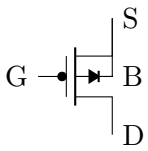
- Speed (→ Timing)
- Power Consumption
- Area
- (Reliability)

Dann: Iterative process with a CAD tools

3.1 Structure and Operation of the MOS Transistor

- p-channel polysilicon-gate MOS
- two operating modes: on/off
- four terminals (Anschlüsse): Gate, Drain, Source and Bulk



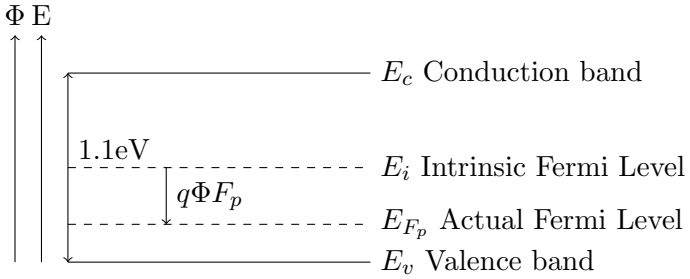


Some Facts:

- Unipolartransistor (nur eine Ladungsträgersorte für Stromfluss verantwortlich)
  PMOS: Löcher → p-Kanal → n-Substrat
  NMOS: Elektronen → n-Kanal → p-Substrat
- Self-aligned (Gate bauen und von oben diffundieren, Verwendung von sehr hoch dotiertem Polysilicon anstatt von Metall)
- möglichst kleiner Kanal (L) → schneller Ladungsaustausch → low latency
- möglichst weites Gate (W) → große Ströme
- Silicon Surface: aktive (Transistor) und Feldregion (z.B. zwischen zwei benachbarten Transistoren auf einem Wafer → Isolation → kein Strom, nur elektrische Felder)
- Body (im Substrat)
- V_T: + für nMos, - für pMos
- Bulk an Source anschliessen: Well Plugs / Substrate Ties: Anschluss des Bulks „oben“.
- STI (Shallow Trench Isolation) in der Feldregion (Isolationsverfahren in der Feldregion, z.B. zwischen den beiden Transistoren eines CMOS-Transistors)

3.2 Threshold Voltage of the MOS Transistor

(metal, insulator, semiconductor)



(p-type semiconductor)

3.2.1 Intrinsic Carrier Concentration[1]

Intrinsische Ladungsträgerkonzentration (Silizium)

$$n_i = 1.45 \cdot 10^{10} \frac{1}{cm^3} \tag{2.1}$$

Im intrinsischen Fall (also undotiert) gilt:

$$p = n$$

Mass Action Law

$$np = n_i^2 \tag{2.2}$$

Im dotierten Halbleiter:

p-Halbleiter	**n-Halbleiter**
$p \approx N_A \gg n_i$	$n \approx N_D \gg n_i$
$n = \frac{n_i^2}{N_A}$	$p = \frac{n_i^2}{N_D}$

Dotierung verschiebt das tatsächlichen Fermi-Niveau E_F um das elektrostatische Potential Φ_F (built-in potential)

$$\Phi_{F_p} = \frac{kT}{q} \ln\left(\frac{n_i}{p}\right) (< 0) \tag{2.3a}$$

$$\Phi_{F_n} = \frac{kT}{q} \ln\left(\frac{n}{n_i}\right) (> 0) \tag{2.3b}$$

Konstanten:

$$V_{\text{Th}} = \frac{kT}{q} \overset{300K}{\approx} 26mV$$
$$k = 1.38 \cdot 10^{-23} \frac{VAs}{K}$$
$$q = 1.602 \cdot 10^{-19} As$$

Materialien des Transistors:
Polysilizium (Gate[2]), SiO_2 (Isolator), Silizium (Substrat)

$$C_{\text{ox}} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad \text{(2.5, Oxidkapazität)}$$

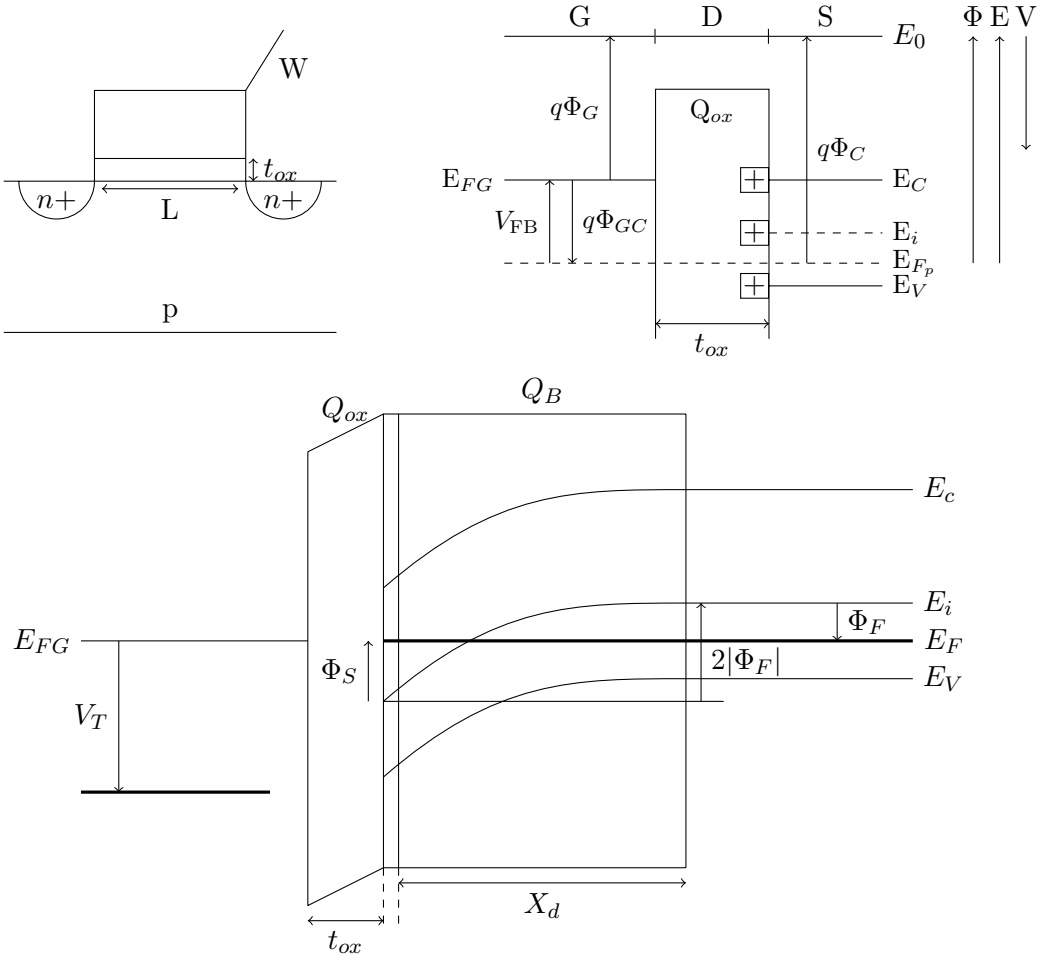
$$\varepsilon_{ox} = \varepsilon_r \cdot 8.85 \cdot 10^{-12} \frac{As}{Vm} \qquad \text{(dielektrische Leitfähigkeit)}$$

$$t_{ox} \leq 5nm \overset{\mathring{A}=10^{-10}m}{=} 50\mathring{A} \qquad \text{(Oxiddicke)}$$

[1] Eigenleitungsträgerdichte

[2] Keine Verwendung von Metall mehr aufgrund von Herstellungsschwierigkeiten im niedrigen μm Bereich

Flatband condition



Große Fläche links: Isolator
Kleine Fläche in der Mitte: Inversion Layer (mobile charge)
Große Fläche rechts: Depletion Layer (exposed fixed charge)

Flatband Voltage (needed to achieve the flatband condition)

$$V_{\mathrm{FB}} = \Phi_{\mathrm{GC}} - \frac{Q_{ox}}{C_{\mathrm{ox}}} \tag{2.6}$$

Work function difference between Gate and Substrate

$$\Phi_{GC} = \Phi_G - \Phi_C$$

Negative Quantity Voltage

$$-\frac{Q_{ox}}{C_{\mathrm{ox}}}$$

Gate Voltage for strong inversion (and to offset induced depletion-layer charge Q_B)

$$-2\Phi_F - \frac{Q_B}{C_{\mathrm{ox}}}$$

Weite der Raumladungszone

$$X_d = \left(\frac{2\varepsilon_{Si} |\Phi_S - \Phi_F|}{qN_A} \right)^{\frac{1}{2}} \tag{2.7}$$

Ladung der Raumladungszone (immobile charge)
(+: n-Halbleiter, -: p-Halbleiter)

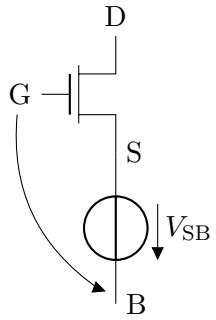
$$Q_B = \pm qNX_d = \pm\sqrt{2qN_A\varepsilon_{Si}|\Phi_S - \Phi_F|} \quad \text{für } |\Phi_S - \Phi_F| \geq 0 \tag{2.8}$$

Maximale Ladung der Raumladungszone im Fall der starken Inversion $\Phi_S = -\Phi_F$:
(+: n-Halbleiter, -: p-Halbleiter)

$$Q_{B_0} = \pm\sqrt{2qN_A\varepsilon_{Si}|-2\Phi_F|} \quad \text{da } \Phi_S = -\Phi_F \tag{2.9a}$$

Falls zusätzlich eine Source-Body Spannung V_{SB} anliegt

$$Q_B = \pm\sqrt{2qN_A\varepsilon_{Si}|-2\Phi_F + V_{SB}|} \begin{array}{ll} \text{nmos} & V_{SB} > 0 \\ \text{pmos} & V_{SB} < 0 \end{array}$$



Threshold Voltage V_T
In Starke Inversion, wenn gilt: $\Phi_S = -\Phi_F \rightarrow \Phi_S - \Phi_F = -|2\Phi_F|$

$$V_{\text{T}} = V_{\text{FB}} - 2\Phi_F - \frac{Q_B}{C_{\text{ox}}} \tag{2.10}$$

$$= \underbrace{\left(\Phi_{GC} - 2\Phi_F - \frac{Q_{B_0}}{C_{\text{ox}}} - \frac{Q_{ox}}{C_{\text{ox}}} \right)}_{=V_{T_0}} - \left(\frac{Q_B - Q_{B_0}}{C_{\text{ox}}} \right) \tag{2.11}$$

$$= V_{T_0} + \gamma \left(\sqrt{V_{\text{SB}} + |2\Phi_F|} - \sqrt{|2\Phi_F|} \right)$$

V_{T_0}: Zero-Bias Threshold Voltage (besteht nur aus technologischen Größen)
γ : body-effect coefficient or body factor:

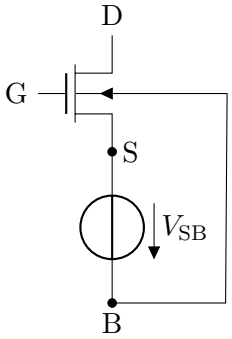
$$\gamma = \frac{1}{C_{\text{ox}}} \sqrt{2q\varepsilon_{Si}N_A} \tag{2.12}$$

Herleitung für γ:

$$-\frac{Q_B - Q_{B_0}}{C_{\text{ox}}} = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{\text{ox}}}\left(\sqrt{|-2\Phi_F| + V_{SB}} - \sqrt{|\Phi_S - \Phi_F|}\right)$$
$$= \underbrace{\frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{\text{ox}}}}_{\to\gamma}\left(\sqrt{V_{SB} + |2\Phi_F|} - \sqrt{|2\Phi_F|}\right) \quad \begin{matrix}\text{nmos} & V_{SB} > 0 \\ \text{pmos} & V_{SB} < 0\end{matrix}$$

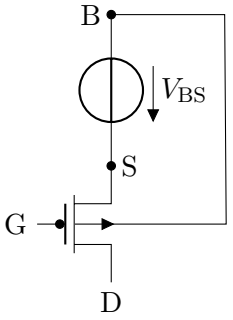
Zusammenfassung:

NMOS (p-type substrate)



$$V_{SB} > 0$$
$$\Phi_{F_p} < 0$$
$$\Phi_S(V_{\text{T}}) = -\Phi_{F_p}$$
$$V_{\text{T}} > 0$$

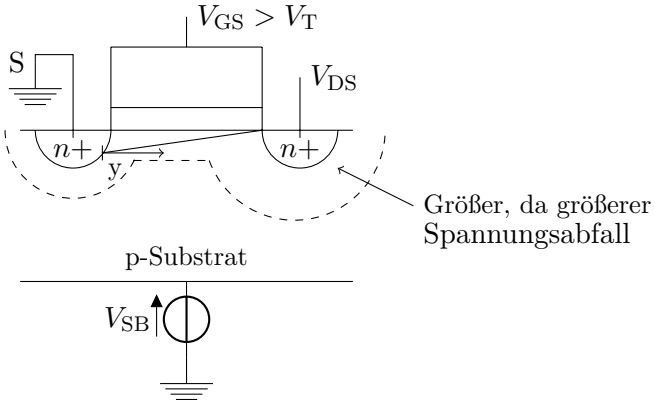
PMOS (n-type substrate)



$$V_{SB} < 0$$
$$\Phi_{F_n} > 0$$
$$\Phi_S(V_{\text{T}}) = -\Phi_{F_n}$$
$$V_{\text{T}} < 0$$

V_{SB} falsch gepolt, hebt auch die Vorspannung der pn-Übergänge in Sperrrichtung auf.
$\Rightarrow$ keine Inversion (kein Transistor mehr)

3.3 First-Order Current-Voltage Characteristics



In basic terms, current is simply charge in motion.

- $0 \leq V(y) \leq V_{\mathrm{DS}}$
- gate-to-channel-voltage: $V_{\mathrm{GS}} - V(y)$
- induced charge per unit area:

$$Q_n(y) = C_{\mathrm{ox}} \cdot (V_{\mathrm{GS}} - V(y) - V_{\mathrm{T}}) \tag{2.13}$$

$$I_{\mathrm{DS}} = Q_n \cdot v \cdot W \tag{2.14}$$

$$v = \mu E \text{ (carrier velocity)} \tag{2.15}$$

μ (carrier mobility) $\left[\frac{cm/s}{V/cm}\right]$

$$E = \frac{dV(y)}{dy}$$

$$I_{\mathrm{DS}} = C_{\mathrm{ox}}(V_{\mathrm{GS}} - V(y) - V_{\mathrm{T}}) \cdot \mu_n E \cdot W$$

$$\Leftrightarrow \; I_{\mathrm{DS}}\, \mathrm{d}y = W \mu_n C_{\mathrm{ox}} \,(V_{\mathrm{GS}} - V(y) - V_{\mathrm{T}})\, \mathrm{d}V$$

$$\text{mit } k' = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} = \mu_n C_{\mathrm{ox}} \text{ (process transconductance parameter)} \tag{2.16}$$

$$\Leftrightarrow \; I_{\mathrm{DS}} \int_0^L \mathrm{d}y = W k' \int_0^{V_{\mathrm{DS}}} (V_{\mathrm{GS}} - V - V_{\mathrm{T}}) dV \tag{2.17a}$$

$$\Leftrightarrow \; I_{\mathrm{DS}} = k' \frac{W}{L}((V_{\mathrm{GS}} - V_{\mathrm{T}})V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2})$$

$$\text{mit } k = k' \frac{W}{L} \text{ (device transconductance parameter)}$$

Linear Region of Operation (only valid up to the pinch-off point):

$$\boxed{I_{\mathrm{DS}} = \frac{k}{2}(2(V_{\mathrm{GS}} - V_{\mathrm{T}})V_{\mathrm{DS}} - V_{\mathrm{DS}}^2)} \tag{2.17b}$$

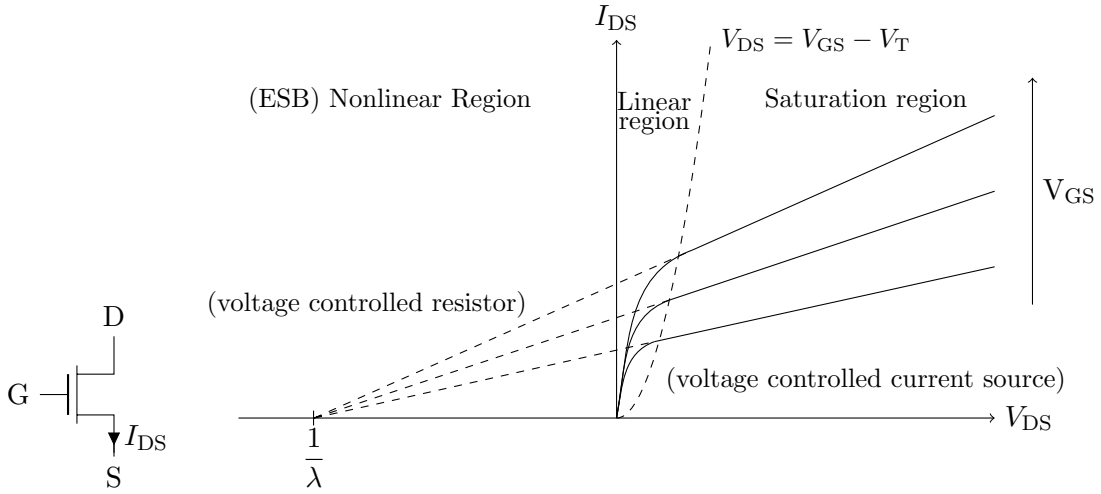
Pinch-off Point (Saturation Voltage):

$$\boxed{V_{\mathrm{Dsat}} = V_{\mathrm{GS}} - V_{\mathrm{T}}} \tag{2.18}$$

V_{Dsat} in (2.17b):

Saturation Region of Operation:

$$\boxed{I_{\mathrm{DS}} = \frac{k}{2}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2} \tag{2.19}$$



Empirical Approximation:

$$I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2.20}$$

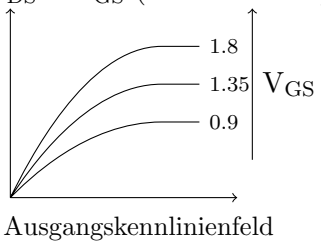
V_{DS}	$>$	V_{GS}	wahrscheinlich Sättigung
V_{DS}	$<$	V_{GS}	wahrscheinlich linearer Bereich
V_{DS}	$=$	V_{GS}	sicher Sättigung

$$I_{DS} = \frac{K}{2}(2(V_{SG} - |V_{T_p}|)V_{SD} - V_{SD}^2)$$
$$I_{DS} = \frac{K}{2}(V_{SG} - |V_{T_p}|)^2$$

- values of V_T can be adjusted with body-bias V_{BS}
- L is usually selected as the minimum value possible
- only practical degree of freedom is the selection of W

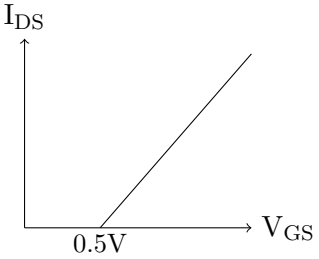
3.4 Derivation of Velocity-Saturated Current Equations

- Bisherige Formeln okay bei long-channel devices ($> 1\mu$m)
- $I_{DS} \sim V_{GS}$ (is more linear)



Ausgangskennlinienfeld

- Aber relativ ungenau bei DSM Devices ($< 0.18\mu$m)
- V_{Dsat} is smaller (0.6V in 0.18μm)



3.4.1 Effect of High Fields

Horizontal Field (between Drain and Source)

$$E_y = \frac{V_{\mathrm{DS}}}{L} \ (\approx 10^5 \frac{V}{cm})$$

weil jetzt: $\mu E \neq v$

Vertical Field (between Gate and Channel)

$$\begin{aligned} E_x &= \frac{V_{\mathrm{DD}}}{t_{ox}} \ (\approx 5 \cdot 10^6 \frac{V}{cm}) \\ \mu_e &= \frac{\mu_0}{1 + \left(\frac{V_{\mathrm{GS}} - V_{\mathrm{T}}}{\Theta \cdot t_{ox}}\right)^{\eta}} \\ \Theta &= 3.6 \cdot 10^6 \frac{V}{cm} \\ \eta &= 1.85 \text{ für } 0.13 \mu m \\ t_{ox} &= 22 \mathring{A} \end{aligned} \tag{2.21}$$

Nominal Mobility in the presence of low fields:

$$\begin{aligned} \mu_0 &= 540 \frac{cm^2}{Vs} \text{ for electrons} \\ V_{\mathrm{GS}} - V_{\mathrm{T}} &= 1.2V - 0.4V = 0.8V \end{aligned}$$

$\mu_e = 270 \frac{cm^2}{Vs}$ $\mu_p = 70 \frac{cm^2}{Vs}$
$v_{sat} = 10^7 \frac{cm}{s}$ $(300K) \sim 8 \cdot 10^6 \frac{cm}{s}$ $(400K)$

Critical Field Values (Sättigung)

$$\begin{aligned} E_{cn} &= 6 \cdot 10^4 \frac{V}{cm} \\ E_{cp} &= 24 \cdot 10^4 \frac{V}{cm} \end{aligned} \tag{2.22}$$

$$v = \begin{cases} \mu_e \cdot \frac{E_y}{1 + \frac{E_y}{E_c}} & E_y < E_c \\ v_{sat} & E_y \geq E_c \end{cases} \tag{2.23a / 2.23b}$$

Durch Umformung des Falls $E_y = E_c$ erhält man:

$$E_c = \frac{2 v_{sat}}{\mu_e}$$

Einsetzen in obige Gleichung ergibt:

$$v = \frac{\mu_e E_c}{2} \tag{2.24}$$

→ Result of our modeling approach!

Current Equations for Velocity-Saturated Devices

aus (2.13), (2.14) und (2.23a) folgt:

$$I_{\mathrm{DS}} = \frac{W}{1 + \frac{E_y}{E_c}} \cdot C_{\mathrm{ox}} \left(V_{\mathrm{GS}} - V_{\mathrm{T}} - V(y) \right) \mu_e E_y$$

Linear Region:

$$I_{\mathrm{DS}} = \frac{W}{L} \frac{\mu_e C_{\mathrm{ox}}}{(1 + \frac{V_{\mathrm{DS}}}{E_c \cdot L})} \left(V_{\mathrm{GS}} - V_{\mathrm{T}} - \frac{V_{\mathrm{DS}}}{2} \right) \cdot V_{\mathrm{DS}} \tag{2.25}$$

Saturation Region (d.h. $v = v_{sat}$):

$$I_{\mathrm{DS}} = W C_{\mathrm{ox}} (V_{\mathrm{GS}} - V_{\mathrm{T}} - V_{\mathrm{DS}}) v_{sat} \text{ mit } v_{sat} = \frac{E_c \mu_e}{2} \tag{2.27}$$

Durch Gleichsetzen von (2.25) und (2.27) erhält man:

$$V_{\mathrm{DSat}} = \frac{(V_{\mathrm{GS}} - V_{\mathrm{T}}) \cdot E_c L}{(V_{\mathrm{GS}} - V_{\mathrm{T}}) + E_c L} \tag{2.28}$$

- V_{DSat} is always lower than the first-order model (which was $V_{\mathrm{Dsat}} = V_{\mathrm{GS}} - V_{\mathrm{T}}$)
- devices saturate faster and deliver less current

$$I_{\mathrm{DS}} = W v_{sat} C_{\mathrm{ox}} \frac{(V_{\mathrm{GS}} - V_{\mathrm{T}})^2}{(V_{\mathrm{GS}} - V_{\mathrm{T}}) + E_c L} \qquad \text{Saturation region} \tag{2.29}$$

long-channel
$E_c L \gg V_{\mathrm{GS}} - V_{\mathrm{T}}$
$I_{\mathrm{DS}} = \frac{W}{2L} \mu_e C_{\mathrm{ox}} (V_{\mathrm{GS}} - V_{\mathrm{T}})^2$
(short-channel ab 0.18/0.13)

short-channel
$E_c L \ll V_{\mathrm{GS}} - V_{\mathrm{T}}$
$I_{\mathrm{DS}} = W v_{sat} C_{\mathrm{ox}} (V_{\mathrm{GS}} - V_{\mathrm{T}})$

Alpha-Power Law

$$I_{\mathrm{DS}} = K_S \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{T}})^{\alpha} \tag{2.30a}$$

$$I_{\mathrm{DS}} = K_L \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{T}}) V_{\mathrm{DS}} \tag{2.30b}$$

$$V_{\mathrm{Dsat}} = \frac{K_S}{K_L} (V_{\mathrm{GS}} - V_{\mathrm{T}})^{\alpha - 1} \tag{2.31}$$

Summary for DSM Devices

First: Decide whether a device is in the linear or saturation region:

$$V_{\mathrm{DS}} \geq \frac{(V_{\mathrm{GS}} - V_{\mathrm{T}}) \cdot E_c L}{(V_{\mathrm{GS}} - V_{\mathrm{T}}) + E_c L} \quad \Rightarrow \text{Saturation}$$
$$V_{\mathrm{DS}} < \frac{(V_{\mathrm{GS}} - V_{\mathrm{T}}) \cdot E_c L}{(V_{\mathrm{GS}} - V_{\mathrm{T}}) + E_c L} \quad \Rightarrow \text{Linear}$$

If we're in saturation region:

$$I_{\mathrm{DS}} = W v_{sat} C_{\mathrm{ox}} \frac{(V_{\mathrm{GS}} - V_{\mathrm{T}})^2}{(V_{\mathrm{GS}} - V_{\mathrm{T}}) + E_c L}$$

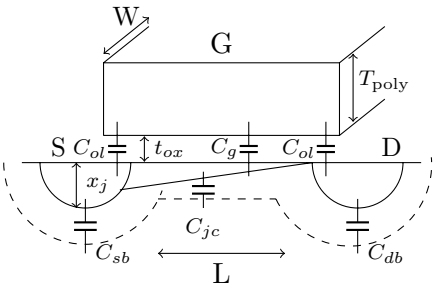
If we're in linear region:

$$I_{\mathrm{DS}} = \frac{W}{L} \frac{\mu_e C_{\mathrm{ox}}}{(1 + \frac{V_{\mathrm{DS}}}{E_c \cdot L})} \left(V_{\mathrm{GS}} - V_{\mathrm{T}} - \frac{V_{\mathrm{DS}}}{2} \right) \cdot V_{\mathrm{DS}}$$

3.5 Capacitances of the MOS transistor

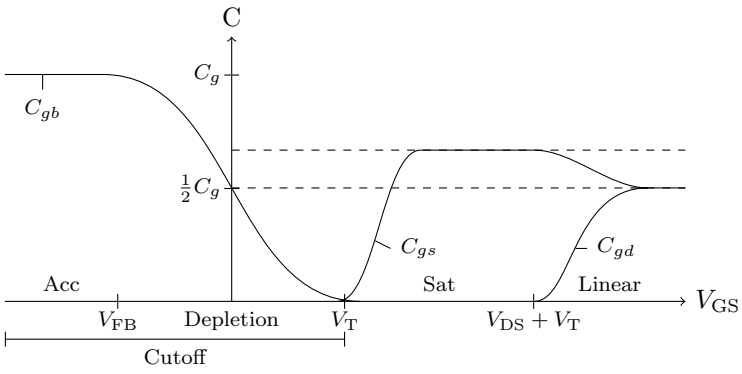
- switching speed limited by the charge / discharge time of internal nodes
- fF / μm: lowercase subscript ($\rightarrow$ Technologiegrößen / spez. Größen)
- total capacitance: uppercase subscript

Nonlinear (voltage dependant) cap



- Thin-Oxide Caps: $C_g(C_{gs}, C_{gd}, C_{gb})$
- Junction Caps: C_{sb}, C_{db}
- Depletion Layer Cap: C_{jc} (associated with Cgb)
- Overlap Cap: C_{ol} (linear)

Thin-Oxide Cap most important



$$C_G = WLC_{\text{ox}} = WL\frac{\varepsilon_{ox}}{t_{ox}} = WC_g \tag{2.34}$$
$$C_g = L\frac{\varepsilon_{ox}}{t_{ox}} = 1.6\frac{fF}{\mu m}$$

C_g ist praktisch eine Konstante, da L und t_{ox} üblicherweise zusammen skaliert werden

pn Junction Cap

- C_{sb}, C_{sd}
- C_{jc}

Leakage Current:

$$I_D = I_S\left(e^{\frac{V_j}{V_{\text{th}}}} - 1\right) \tag{2.35}$$
$$I_D(V_j < 0) = -I_S \tag{2.36}$$

In normal operation, all pn junctions are reverse-biased.

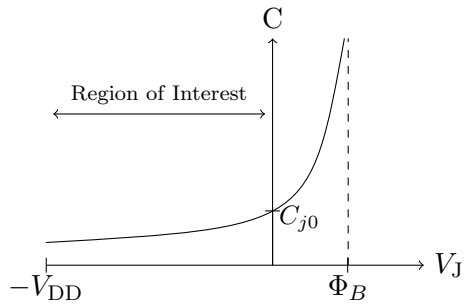
Built-in junction potential:
Trägerdichte nach Boltzmann-Verteilung

$$N_D = n = n_i \exp\left(\frac{q\Phi_{Fn}}{kT}\right)$$
$$\Phi_{Fn} = \frac{kT}{q}\ln\left(\frac{n}{n_i}\right) \quad (>0)$$
$$N_A = p = n_i \exp\left(\frac{-q\Phi_{Fp}}{kT}\right)$$
$$\Phi_{Fp} = \frac{kT}{q}\ln\left(\frac{n_i}{p}\right) \quad (<0)$$
$$\Phi_B = \frac{kT}{q}\ln\left(\frac{N_D N_A}{n_i^2}\right) = \Phi_{Fn} - \Phi_{Fp} \tag{2.37}$$

Breite der Raumladungszone (depletion zone)

$$X_d = \sqrt{\frac{2\varepsilon_{Si}}{q}\Phi_B\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$$

Gespeicherte Ladung



Zero-Bias Junction Cap:

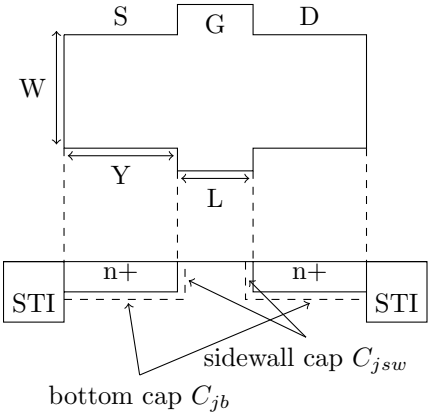
$$C_{j0} = \frac{\varepsilon_{Si}}{X_d} = \sqrt{\frac{\varepsilon_{Si}q}{2\Phi_B}\frac{N_A N_D}{N_A+N_D}} \tag{2.39}$$

bei einem abrupten pn Übergang:

$$\approx \sqrt{\frac{\varepsilon_{Si}qN_A}{2\Phi_B}} \tag{2.40}$$

$$C_J = \frac{C_{j0}A}{\left(1-\frac{V_J}{\Phi_B}\right)^m} \tag{2.38}$$

V_J hängt ab von V_{BS}, V_{BD}



$$A_b = WY$$
$$A_{sw} = Wx_j$$

$$C_J = \frac{C_{jb}A_b}{\left(1-\frac{V_J}{\Phi_{Bb}}\right)^{mj}} + \frac{C_{jsw}A_{sw}}{\left(1-\frac{V_J}{\Phi_{Bsw}}\right)^{mjsw}} \tag{2.41}$$

bei einem abrupten pn Übergang:

$$\approx \frac{C_{jb}(A_b+A_{sw})}{\left(1-\frac{V_J}{\Phi_B}\right)^{mj}} \tag{2.42}$$

$V_J \in [-V_{DD}, 0]$, Nenner $\in [1,2]$

In digital circuitry, the voltage switches from high-to-low and vice-versa.
⇒ Equivalent, voltage-independent capacitance C_{eq}:

$$C_{eq} = \frac{Q_j(V_2) - Q_j(V_1)}{V_2 - V_1} = \frac{\Delta Q}{\Delta V}$$

$$\Delta Q = \int_{V_1}^{V_2} C(V)\mathrm{d}V = \int_{V_1}^{V_2} C_{jb}\left(1 - \frac{V}{\Phi_B}\right)^{-m} \mathrm{d}V$$

$$C_{eq} = -\frac{C_{jb}\Phi_B}{(V_2 - V_1)(1-m)}\left[\left(1 - \frac{V_2}{\Phi_B}\right)^{1-m} - \left(1 - \frac{V_1}{\Phi_B}\right)^{1-m}\right]$$

bei einem abrupten pn Übergang gilt $m = 0.5$ und damit:

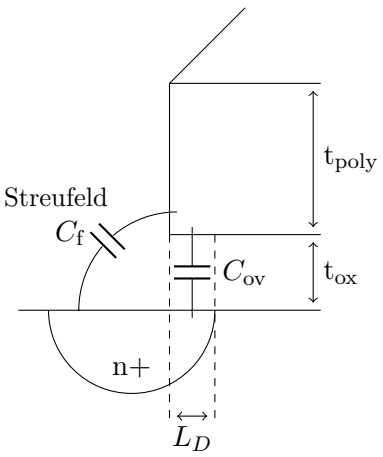
$$K_{eq} = \frac{C_{eq}}{C_{jb}} = \frac{-2\Phi_B^{\frac{1}{2}}}{V_2 - V_1}((\Phi_B - V_2)^{\frac{1}{2}} - (\Phi_B - V_1)^{\frac{1}{2}}) \tag{2.43}$$

$$\begin{aligned} C_J &= K_{eq}(C_{jb}WY + C_{jb}x_jW) \\ &= K_{eq}C_{jb}(Y + x_j)W \qquad (2.44) \\ &= C_jW \qquad (2.45) \end{aligned}$$

Beim Switching gilt: $K_{eq} \approx 0.75$

NMOS	$K_{eq}(V_{\mathrm{SB}} = 0) = 1.0$	$K_{eq}(V_{\mathrm{J}} = -V_{\mathrm{DD}}) = 0.5$
PMOS	$K_{eq}(V_{\mathrm{BS}} = 0) = 1.0$	$K_{eq}(V_{\mathrm{J}} = -V_{\mathrm{DD}}) = 0.5$

Overlap Cap:



$$C_{ol} = C_{ov} + C_f \tag{2.46}$$

$$C_f = \frac{2\varepsilon_{ox}}{\pi}\ln\left(1 + \frac{T_{poly}}{t_{ox}}\right) \quad \text{(fringe cap, 2.47)}$$

$$C_{ov} = C_{\mathrm{ox}} \cdot L_D \quad \text{(overlap cap)}$$

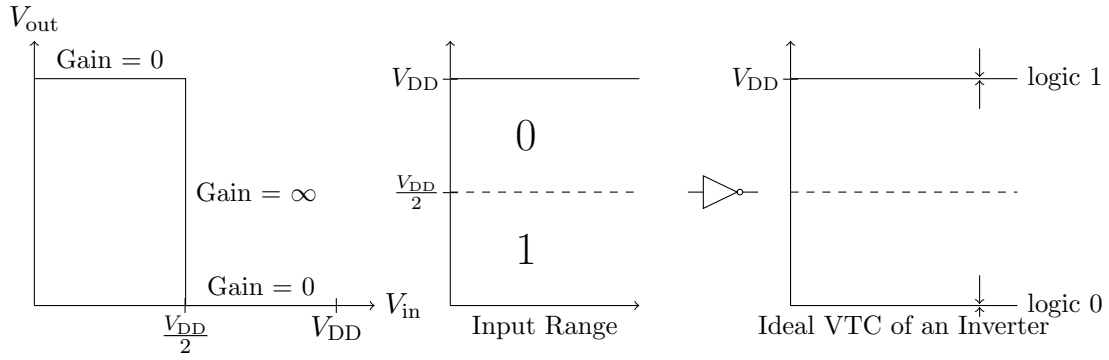
L_D lateral diffusion

4 MOS Inverter Circuits

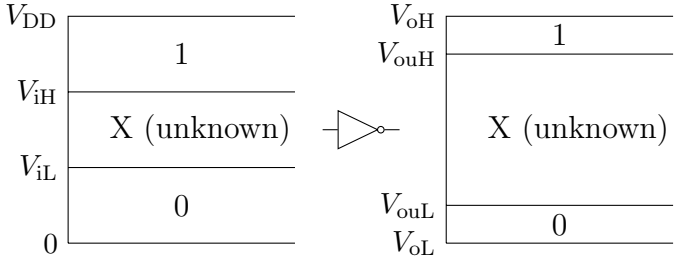
- static vs. dynamic circuitry
  - all nodes of a static gate will have resistive paths to V_{DD} or GND

  - the value of one or more nodes in a dynamic circuitry is based on stored charge on a capacitor
- periodic clock signal
  - combinational logic
  - sequential logic
  - to load elements, so called transmission gates, or transfer gates
- static inverters
  - VTC, voltage transfer characteristics
  - noise margin
  - inverter configurations
  - delay models

4.1 Voltage Transfer Characteristics



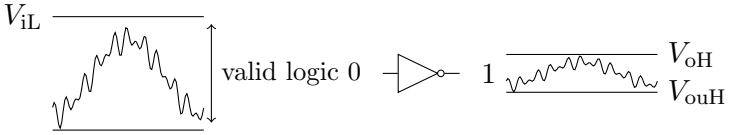
high gain region is required by all useful logic gates to regenerate high and low logic values if there is noise in the system.
low gain regions exhibits large noise immunity.



Practical VTC

- Switching Point $V_S : V_{out} = V_{in}$
- uncertain region

- attenuating noise in low gain regions (damping noise out of a inverter chain)



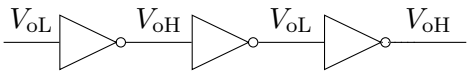
Effect of noise at logic gate input on the output

4.2 Noise Margin Definitions

- unwanted variations of voltages or current at logic nodes
- if the noise amplitude at the input of any logic circuit is smaller than the noise margin, it is attenuated from input to output (Kurz: Dämpfung des Rauschens, keine Veränderung des Wertes)
- noise does not accumulate from one logic gate stage to the next, as it does in analog systems
- variations due to
  - manufacturing tolerances
  - temperature changes
  - power supply variations
  - electrical loading
- noise metrics
  - SSNM (`single source/stage noise margin`)
  - MSNM (`multiple source/stage noise margin`)
- robustness of a gate
  - ability to operate properly in the presence of noise
    - how much noise can be applied before the gate failes?
    - how much noise actually couples into the gate?[3]

4.2.1 Single-Source Noise Margin

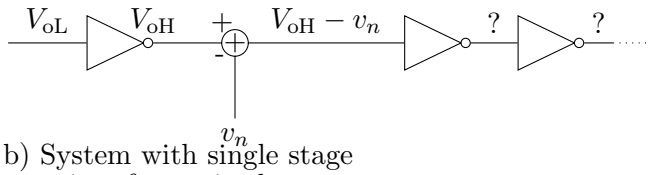
- single noise source
- effect on downstream logic gates



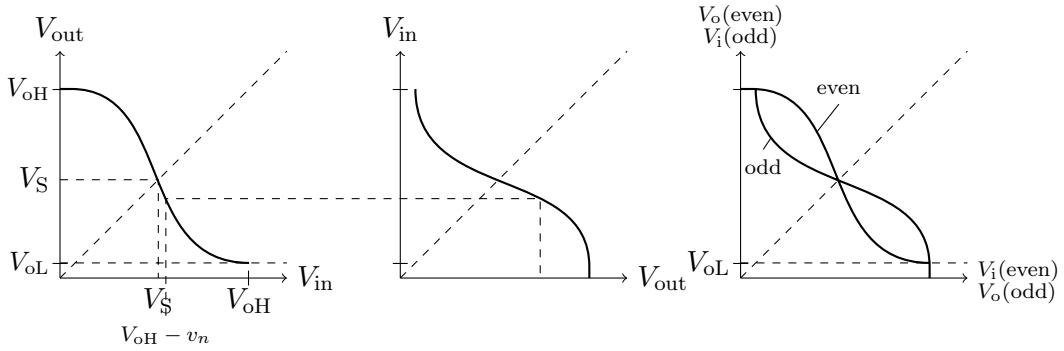
a) Noiseless System

- largest noise level v_n in a single stage that allowes subsequent stages to recover their proper value (the regenerative property)

[3] Umgebung ?



b) System with single stage noise of magnitude v_n



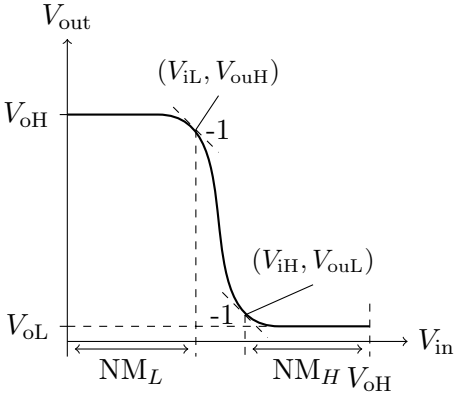
$$\text{SSNM}_H = V_{oH} - V_S \qquad V_S \neq V_T$$
$$\text{SSNM}_L = V_S - V_{oL}$$

4.2.2 Multiple-Source Noise Margin (MSNM)

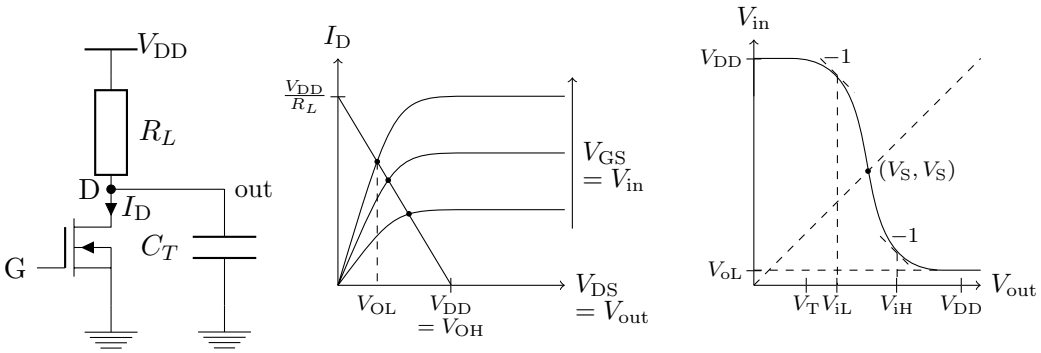
- noise tends to be added to all nodes

$$V_{out} = f(V_{in} + v_n) = f(V_{in}) + v_n \frac{\delta V_{out}}{\delta V_{in}} + \ldots$$

  - amplified for $\left|\frac{\delta V_{out}}{\delta V_{in}}\right| > 1$
  - attenuated for $\left|\frac{\delta V_{out}}{\delta V_{in}}\right| < 1$



4.3 Resistive Load Inverter Design



a) Symbol b) load line c) VTC

Funktionsweise:
NMOS device off: The resistor pulls the output high to V_{oH}.
NMOS device on: It forms a resistive divider with the pull-up device and produces a low output V_{oL}.
The design parameters are: R_L, $\frac{W}{L}$ and V_{DD} (wobei letzteres meistens Technologieparameter und damit schon vorgegeben)

$V_{oH}, V_{oL}, V_{iH}, V_{iL}, V_S(\lambda = 0)$

$$I_{DS} = \frac{V_{DD} - V_{oL}}{R_L} = I_R \tag{4.4}$$

$$V_{oH} = V_{DD} \tag{4.5}$$

$$V_{oL} : I_R = I_{DS}(I_{in}) \tag{4.6a}$$

$$\frac{V_{DD} - V_{oL}}{R_L} = \frac{W_N}{L_N} \frac{\mu C_{ox}}{(1 + \frac{V_{oL}}{E_c L})} \left(2(V_{oH} - V_T)V_{oL} - V_{oL}^2\right) \frac{1}{2} \tag{4.6b}$$

$$V_{oL}^2 - 2\left(\frac{1}{kR_L} + V_{DD} - V_T\right) V_{oL} + \frac{2V_{DD}}{kR_L} = 0 \tag{4.6c}$$

Lösen per Mitternachtsformel : $ax^2 + bc + c = 0$

$$x_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$\sqrt{1 - x} = 1 - \frac{x}{2} \text{ für } |x| \leq 1$$

$$x_{1,2} = \frac{-b \pm b - \frac{4ac}{2b}}{2a} = -\frac{ac}{ba} = -\frac{c}{b}$$

$$x_{1,2} = -\frac{2V_{DD}}{kR_L} \frac{1}{-2\left(\frac{1}{kR_L} + V_{DD} - V_T\right)}$$

$$= \frac{V_{DD}}{1 + kR_L(V_{DD} - V_T)} = V_{oL} \tag{4.6d}$$

Discussion of 4.6d

$V_{\mathrm{oL}} \downarrow$ by $\frac{W}{L} \uparrow$ or $R_{\mathrm{L}} \uparrow$ (at the expense of area)

$R_{\mathrm{L}} \uparrow \Rightarrow t_r \uparrow$, $k \uparrow \Rightarrow t_f \downarrow$

$V_{\mathrm{oL}} \downarrow$ und $k \uparrow \Rightarrow$ Power $\uparrow$ Power $= I \cdot V = \left(\frac{V_{\mathrm{DD}}}{R_{\mathrm{L}}}\right) V_{\mathrm{DD}}$

$R_{\mathrm{L}} \uparrow \Rightarrow$ Power $\downarrow$ ultimately: Noise margin traded off by te choise of K an R_{L}

Bestimmung von $V_{\mathrm{iL}}, V_{\mathrm{iH}}$ mit $\frac{\delta V_{\mathrm{out}}}{\delta V_{\mathrm{in}}} = -1$

$$V_{\mathrm{in}} = V_{\mathrm{iL}}$$

$$V_{\mathrm{out}} \leq V_{\mathrm{DD}}$$

$$I_{\mathrm{R}} = I_{\mathrm{DS}}(\mathrm{sat}) \tag{4.8a}$$

$$\frac{V_{\mathrm{DD}} - V_{\mathrm{out}}}{R_{\mathrm{L}}} = \frac{W v_{sat} C_{ox} (V_{\mathrm{in}} - V_{\mathrm{T}})^2}{\cancel{(V_{\mathrm{in}} - V_{\mathrm{T}})} + E_c L} \tag{4.8}$$

$$\text{mit } v_{\mathrm{sat}} = \frac{\mu E_c}{2}$$

$$\text{und } k = \frac{W}{L} \mu_n C_{\mathrm{ox}}$$

$$\frac{1}{R_{\mathrm{L}}} \left(\frac{\delta V_{\mathrm{out}}}{\delta V_{\mathrm{in}}}\right) = k(V_{\mathrm{in}} - V_{\mathrm{T}}) \quad - \frac{1}{R_{\mathrm{L}}}, \text{ Faktor 2 ?}$$

$$V_{\mathrm{iL}} = V_{\mathrm{T}} + \frac{1}{k R_{\mathrm{L}}} = \mathrm{NM}_L \tag{4.8b}$$

Bewertung

$\mathrm{NM}_L \uparrow \Leftarrow (K \downarrow \text{ and } R_{\mathrm{L}} \downarrow) \Rightarrow \underbrace{V_{\mathrm{oL}} \uparrow}_{\text{not desirable}}$

V_{iL} and V_{oL} shift in the same direction

R_{L} and $\frac{W}{L}$ will most likely be controlled by V_{oL} (V_{oL} specified by spec)

$$V_{\text{ouH}} = V_{\text{DD}} = \frac{KR_{\text{L}}}{2}(V_{\text{iL}} - V_{\text{T}})^2$$

$$V_{\text{in}} = V_{\text{iH}} \Rightarrow \text{ linear region}$$

$$I_{\text{DS}}(\text{lin}) = I_{\text{R}}$$

$$\frac{W}{L}\frac{\mu_n C_{ox}}{1 + \cancel{\frac{V_{\text{out}}}{E_c L}}}\left((V_{\text{in}} - V_{\text{T}})V_{\text{out}} - \frac{V_{\text{out}}^2}{2}\right) = \frac{V_{\text{DD}} - V_{\text{out}}}{R} \tag{4.8c}$$

$$V_{\text{IH}} = V_{\text{T}} + 2V_{\text{out}} - \frac{1}{KR_{\text{L}}}(V_{\text{in}} = V_{\text{IH}}) \tag{4.8d}$$

$$(4.8\text{d}) \text{ in } (4.8\text{c}) \Rightarrow (4.8\text{e}) \wedge (4.8\text{d})$$

$$\frac{KR_{\text{L}}}{2}(3V_{\text{out}}^2 - \cancel{\frac{2V_{\text{out}}}{kR_{\text{L}}}} = V_{\text{DD}} - \cancel{V_{\text{out}}}$$

$$V_{\text{out}}^2 = \frac{2V_{\text{DD}}}{2KR_{\text{L}}}(\text{in } 4.8\text{d})$$

$$V_{\text{IH}} = V_{\text{T}} + \sqrt{\frac{8V_{\text{DD}}}{3kR_{\text{L}}}} - \frac{1}{kR_{\text{L}}} \tag{4.8f}$$

$KR_{\text{L}} \uparrow \Rightarrow V_{\text{iH}} \downarrow \Rightarrow NM_H \uparrow \Rightarrow \underbrace{t_r \uparrow (Power \uparrow)}_{desired}$

$V_{\text{oL}} = 4.8e(V_{\text{in}} = V_{\text{IH}})$

$V_{\text{S}} = V_{\text{in}} = V_{\text{out}}$

$V_{\text{DS}} = V_{\text{GS}} = I_{\text{R}}$

$$\frac{W v_{sat} C_{ox}(V_{\text{S}} - V_{\text{T}})^2}{(V_{\text{S}} - V_{\text{T}}) + E_c L} = \frac{V_{\text{DD}} - V_{\text{S}}}{R_{\text{L}}} \tag{4.9}$$

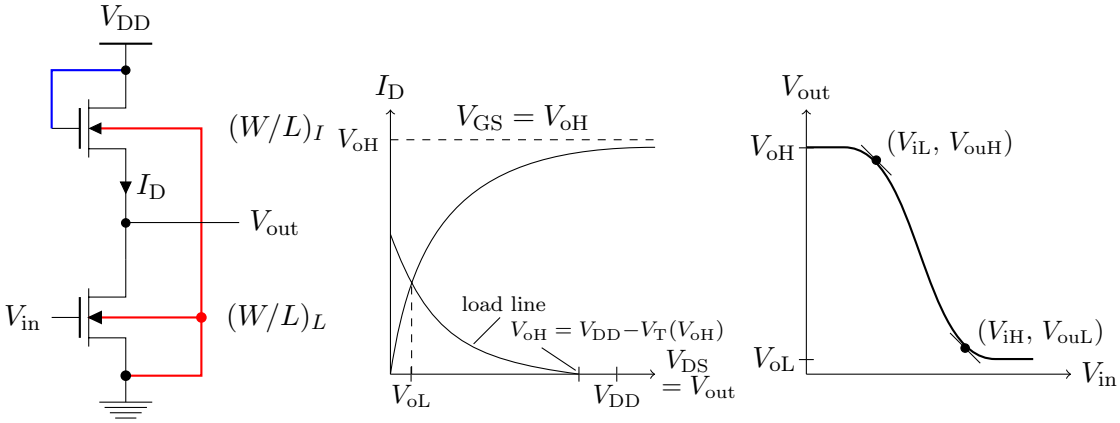
- iterative guess of $\frac{V_{\text{DD}}}{2}$
- solved directly: Übung

4.4 NMOS Transistors as Load Devices

- Transistor area is less than $\frac{1}{100}$ area of resistive load
- resistive load produces a low rise time

4.4.1 Saturated Enhancement Load ($V_{\text{GS}} = V_{\text{DS}}$)

→ can only operate in saturation or cut-off



a) enhancement-loaded inverter, saturated load

b) drain characteristic and load line

c) VTC

Ratioed Inverter (it's crucial) (vs ratioless)

- relative sizes of the two transistors determine the output voltage
- nur funktionsfähig wenn $V_{oL} \ll V_T$
- specific ratio between PU and PD devices

$$K_R = \frac{K_{\text{invert}}}{K_{\text{load}}} = \frac{k'(\frac{W}{L})_I}{k'(\frac{W}{L})_L} = \frac{(\frac{W}{L})_I}{(\frac{W}{L})_L} \tag{4.10}$$

- $V_{oL} \approx 5\% \cdot V_{DD}$
- Threshold Voltage

$$V_{TL} = V_{T0} + \gamma \left(\sqrt{V_{SB} + 2|\Phi_F|} - \sqrt{2|\Phi_F|} \right) \tag{4.11}$$

- $V_{SB} = V_{oH} = V_{DD} - V_T$
-

$$\begin{aligned} V_{oH} &= V_{DD} - V_T(V_{oH}) \\ &= V_{DD} - \left(V_{T0} + \gamma \left(\sqrt{V_{SB} + 2|\Phi_F|} - \sqrt{2|\Phi_F|} \right) \right) \end{aligned} \tag{4.12}$$

- V_{oL}: $I_{DI}(\text{lin}) = I_{DL}(\text{sat})$
- When PU in saturation and PD in linear region:

$$\frac{W_I}{L_I} \frac{\mu_n C_{ox}}{1 + \frac{V_{out}}{E_{CN} L_I}} \left[(V_{in} - V_{TI}) V_{out} - \frac{V_{out}^2}{2} \right] = \frac{W_L V_{sat} C_{ox} \left(V_{DD} - V_{out} - V_{TL} \right)^2}{(V_{DD} - V_{out} - V_{TL}) + E_{CN} L_L}$$

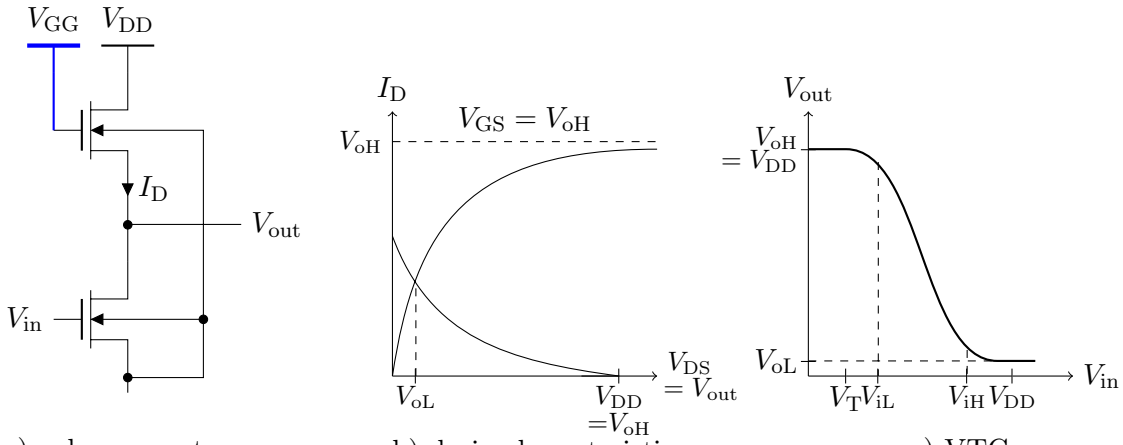
- significant dc-power dissipation when output low

4.4.2 Linear Enhancement Load

- Connect the Gate of the load transistor to a dc voltage $V_{GG} > V_{DD}$ to increase V_{oH}

$$V_{GG} > V_{DD} + V_{TL}(V_{DD}) \tag{4.13}$$

  $\rightarrow$ load devices can pull the output up to V_{DD}
- load devices always in linear region since $V_{DS} < V_{GS} - V_{TL}$ (for long-channel devices)
  $\Rightarrow$ linear load (or non-saturated load or triode load)
  (false for short-channel devices)



a) enhancement-loaded inverter, linear load

b) drain characteristic and load line

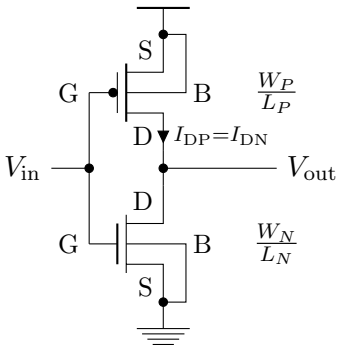
c) VTC

- extra voltage source ($\rightarrow V_{GG}$) with additional interconnects
- K_R is larger than for a saturated enhancement load
- dc power dissipation when output low
- rarely, if ever, used as stand-alone gates

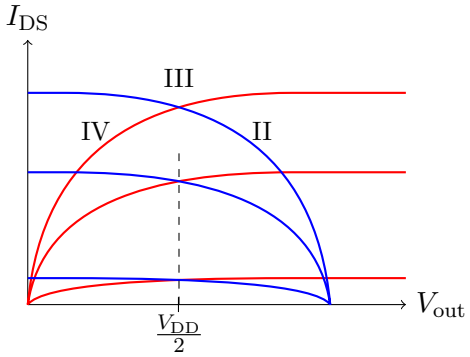
4.4.3 Complementary MOS (CMOS) Inverters

- High noise margins
- Low power dissipation

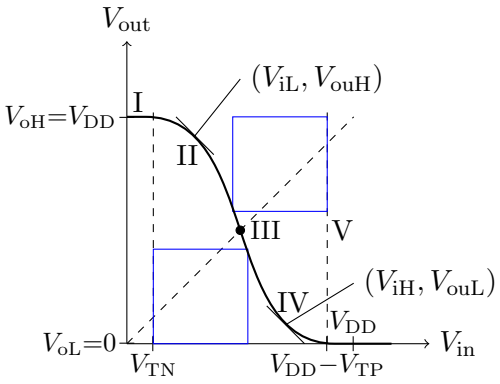
DC Analysis of CMOS Inverter



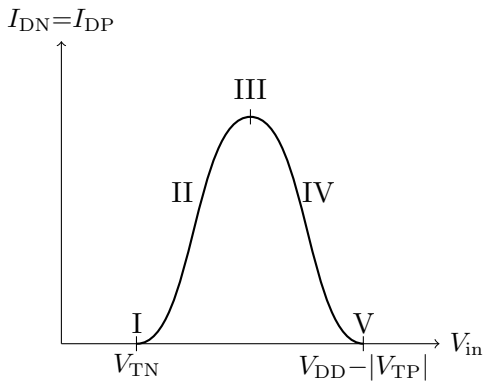
a) Inverter



b) load line



c) VTC



d) Current (Diode Transfer Curve)

	V_{in}	NMOS	PMOS
I	$0 \leq V_{in} \leq V_{TN}$	off	lin
II	$V_{TN} \leq V_{in} \leq V_{out} - \lvert V_{TP}\rvert$	sat	lin
III	$V_{out} - \lvert V_{TP}\rvert \leq V_{in} \leq V_{out} + V_{TN}$	sat	sat
IV	$V_{out} + V_{TN} \leq V_{in} \leq V_{DD} - \lvert V_{TP}\rvert$	lin	sat
V	$V_{DD} - \lvert V_{TP}\rvert \leq V_{in} \leq V_{DD}$	lin	off

$\left.\begin{array}{l} V_{oH} = V_{DD} \\ V_{oL} = 0V \end{array}\right\}$ large noise margins

A completely symmetrical VTC is obtained if $V_{TP} = -V_{TN}$ and $K_p = K_N$.
The gate is static in that there is always a conducting path from the output to V_{DD} xor Gnd.

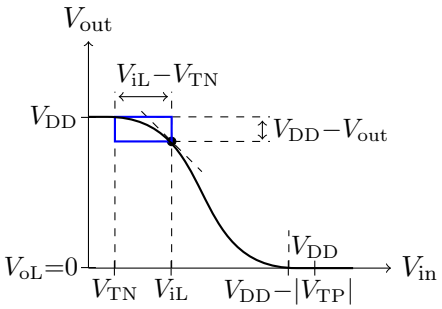
- subthreshold currents
- leakage currents
  $\Rightarrow$ quiescent power dissipation [nW]

Bereich III

$$\begin{aligned}
\sqrt{\chi}(V_S - V_{TN}) &=_{(} \pm (V_{DD} - V_S - |V_{TP}|) \\
\chi &= \sqrt{\frac{\frac{W_N}{E_{CN}L_N}}{\frac{W_P}{E_{CP}L_P}}} \\
&= \sqrt{\frac{W_N \mu_n}{W_P \mu_p}} \qquad (4.15) \\
E_C &= \frac{2V_{sat}}{\mu_e} \\
\chi \uparrow &\Rightarrow V_S \downarrow
\end{aligned}$$

Increasing the size of the NMOS device → Left-Shift of the VTC
Increasing the size of the PMOS device → Right-Shift of the VTC
⇒ Skewed Inverter
aus (4.17):

$$V_{iL}\left(1 + \frac{K_N}{K_P}\right) = 2V_{out} - V_{DD} - |V_{TP}| + \frac{K_N}{K_P}V_{TN}$$



An der Stelle (V_{iL}, V_{ouH}) ist die Steigung $V'_{out}(V_{in}) = -1$.

$$\begin{aligned}
\underbrace{(V_{iL} - V_{TN})}_{x} &= -\underbrace{\frac{K_N}{K_P}}_{\alpha}(V_{iL} - V_{TN}) - 2\underbrace{(V_{DD} - V_{out})}_{y} \\
&\quad + \underbrace{(V_{DD} - (V_{TN} + |V_{TP}|))}_{z} \qquad (4.17') \\
\chi^2 &= \alpha \qquad (4.15) \\
&\text{aus (4.16) :} \\
\frac{1}{2}\frac{K_N}{K_P}(V_{iL} - V_{TN})^2 &= (V_{DD} - V_{out})\frac{1}{2}[-(V_{DD} - V_{out}) \\
&\quad + 2(V_{DD} - (V_{TN} + |V_{TP}|)) - 2(V_{iL} - V_{TN})] \qquad (4.16')
\end{aligned}$$

damit :

$$2y = z - x(1+\alpha) \tag{4.17"}$$

$$\alpha x^2 = y(2z - 2x - y) \tag{4.16"}$$

(4.17") in (4.16") :

$$\begin{aligned}
\alpha x^2 &= \frac{1}{2}(z - x(1+\alpha))(2z - 2x - \frac{1}{2}z + \frac{x}{2}(1+\alpha)) \\
&= \frac{1}{4}(z - x(1+\alpha))(3z - x(3-a)) \\
4\alpha x^2 &= 3z^2 + x^2(3 + 2\alpha - \alpha^2) - xz(3 + 3\alpha + 3 - \alpha) \\
3z^2 &= x^2(\alpha^2 + 2\alpha - 3) + 2xz(3+\alpha) \qquad (1) \\
3z^2 &= x^2(\alpha - 1)(\alpha + 3) + 2xz(\alpha + 3) \qquad (1')
\end{aligned}$$

$$\begin{aligned}
K_N = K_P &\Rightarrow \alpha = 1 \\
|V_{\mathrm{TP}}| = V_{\mathrm{TN}} &\Rightarrow z = V_{\mathrm{DD}} - 2V_{\mathrm{TN}} \\
&\Rightarrow \text{symmetrische VTC } (V_{\mathrm{iL}} + V_{\mathrm{iH}} = V_{\mathrm{DD}})
\end{aligned}$$

aus (1') folgt :

$$\begin{aligned}
x &= \frac{3}{8}z \\
V_{\mathrm{iL}} &= \frac{2}{8}V_{\mathrm{DD}} + V_{\mathrm{TN}} - \frac{3}{8}V_{\mathrm{TN}} \cdot 2 = \frac{1}{4}\left(\frac{3}{2}V_{\mathrm{DD}} + V_{\mathrm{TN}}\right) \\
V_{\mathrm{iH}} &= V_{\mathrm{DD}} - V_{\mathrm{iL}} = \frac{1}{4}\left(\frac{5}{2}V_{\mathrm{DD}} - V_{\mathrm{TN}}\right)
\end{aligned}$$

$$
\begin{aligned}
K_N = K_P \Rightarrow \alpha &= 1 \\
z &= V_{\mathrm{DD}} - (V_{\mathrm{TN}} + |V_{\mathrm{TP}}|) \\
V_{\mathrm{iL}} + V_{\mathrm{iH}} &= 2V_{\mathrm{S}} \\
V_{\mathrm{S}} &= V_{\mathrm{TN}} + \frac{V_{\mathrm{DD}} - (V_{\mathrm{TN}} + |V_{\mathrm{TP}}|)}{2} \\
V_{\mathrm{iL}} + V_{\mathrm{iH}} &= 2V_{\mathrm{TN}} + V_{\mathrm{DD}} - V_{\mathrm{TN}} - |V_{\mathrm{TP}}| = V_{\mathrm{DD}} + V_{\mathrm{TN}} - |V_{\mathrm{TP}}| \\
&\Rightarrow \text{skewed VTC } (V_{\mathrm{iL}} + V_{\mathrm{iH}} = V_{\mathrm{DD}} + V_{\mathrm{TN}} - |V_{\mathrm{TP}}|)
\end{aligned}
$$

aus (1') folgt :

$$
\begin{aligned}
x &= \frac{3}{8}z \\
V_{\mathrm{iL}} &= V_{\mathrm{TN}} + \frac{3}{8}V_{\mathrm{DD}} - \frac{3}{8}V_{\mathrm{TN}} - \frac{3}{8}|V_{\mathrm{TP}}| = \frac{1}{8}\left(3V_{\mathrm{DD}} + 5V_{\mathrm{TN}} - 3|V_{\mathrm{TP}}|\right) \\
V_{\mathrm{iH}} &= V_{\mathrm{DD}} + V_{\mathrm{TN}} + |V_{\mathrm{TP}}| - V_{\mathrm{iL}} = \frac{1}{8}\left(5V_{\mathrm{DD}} + 3V_{\mathrm{TN}} - 5|V_{\mathrm{TP}}|\right)
\end{aligned}
$$

aus (1') :

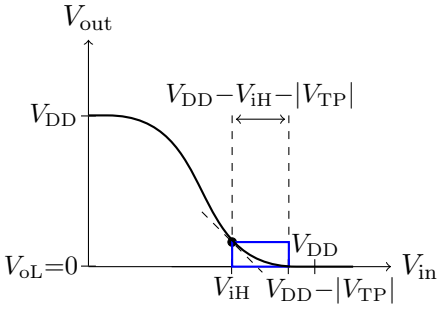
$$
\begin{aligned}
x^2(a+3)(a-1) + 2x(3+a)z &= 3z^2 \\
x^2 + 2x\frac{z}{(a-1)} + \left(\frac{z}{a-1}\right)^2 &= \frac{3z^2}{(a-1)(a+3)} + \left(\frac{z}{a-1}\right)^2 \\
\left(x + \frac{z}{a-1}\right)^2 &= \frac{3z^2(a-1) + z^2(a+3)}{(a-1)^2(a+3)} \\
&= \left(\frac{2z}{a-1}\right)^2 \frac{a}{a+3} \\
x &= -\frac{z}{a-1} \overset{(+)}{} \frac{2z}{a-1}\sqrt{\frac{a}{a+3}} \\
&= \frac{z}{a-1}\left(2\sqrt{\frac{a}{a+3}} - 1\right)
\end{aligned}
$$

für $a = 1$ nach l'Hopital $x = \frac{3}{8}z$ q.e.d.

Bereich IV

$$
V_{\mathrm{out}}\left((V_{\mathrm{iH}} - V_{\mathrm{TN}}) - \frac{V_{\mathrm{out}}}{2}\right) = \frac{K_N}{K_P}\frac{1}{2}(V_{\mathrm{DD}} - |V_{\mathrm{TP}}| - V_{\mathrm{iH}})^2 \tag{4.18}
$$

$$
V_{\mathrm{iH}}\left(1 + \frac{K_P}{K_N}\right) = 2V_{\mathrm{out}} + V_{\mathrm{TN}} + \frac{K_P}{K_N}(V_{\mathrm{DD}} - |V_{\mathrm{TP}}|) \tag{4.19}
$$



$$-(V_{\text{DD}} - |V_{\text{TP}}| - V_{\text{iH}}) = 2\underbrace{V_{\text{out}}}_{y} - \underbrace{(V_{\text{DD}} - (V_{\text{TN}} + |V_{\text{TP}}|))}_{z} + \underbrace{\frac{K_P}{K_N}}_{\alpha}\underbrace{(V_{\text{DD}} - |V_{\text{TP}}| - V_{\text{iH}})}_{x}$$

$$z = 2y + x(1+\alpha) \tag{4.19"}$$

$$ax^2 = y(-2x + 2z - y) \tag{4.18"}$$

strukturgleich mit (4.16") und (4.17")

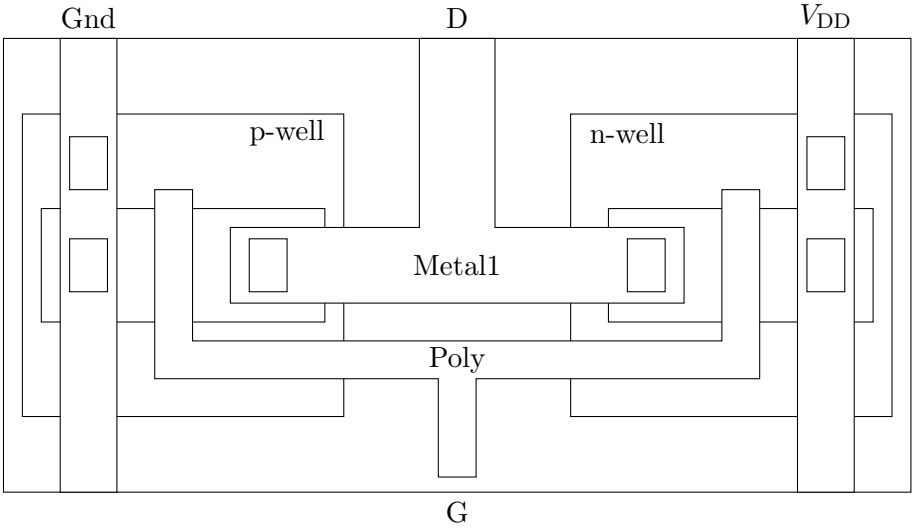
$$\text{l'Hopital } \frac{2\sqrt{\frac{a}{a+3}} - 1}{a-1} = \frac{0}{0}$$

$$\overset{a=1}{\Rightarrow} 2\frac{1}{2}\frac{1}{\sqrt{\frac{a}{a+3}}}\frac{a+3-a}{(a+3)^2}$$

$$= 3(a+3)^{-\frac{3}{2}}a^{-\frac{1}{2}} = \frac{3}{8}$$

4.5 Layout design of CMOS Inverter

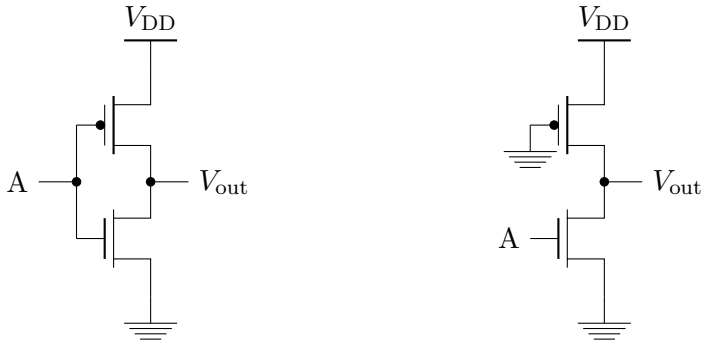
- Layers: Metal1, Poly, Contact, n+, p+, n-well, p-well



- well plugs
- metal-to-poly (not shown here)
- 4 contacts
- L, W, **A**rea **S**ource, **A**rea **D**rain, **P**erimeter **S**ource, **P**erimeter **D**rain

4.6 Pseudo-NMOS Inverters

- sometimes high fanin gate needed
- saturated enhancement NMOS load inverter suffers from low V_{oH}
- linear enhancement NMOS load inverter needs two voltage supplies
- But both have one advantage: only one load required, regardless of the number of inputs
  (contrary to twice as many transistors in push-pull arrangement is standard CMOS)



a) CMOS b) Pseudo NMOS Inverter

b) will fight the NMOS transistor when it is on

$\Rightarrow$ ratioed inverter (V_{oL})
power dissipation during output low
smaller area for multi-img gates

$$V_{\mathrm{oH}} = V_{\mathrm{DD}} \tag{4.20}$$

$$V_{\mathrm{oL}} : I_{\mathrm{DP}}(\mathrm{sat}) = I_{\mathrm{DN}}(\mathrm{lin})$$

$$\frac{W_P v_{sat} C_{\mathrm{ox}} (V_{\mathrm{DD}} - |V_{\mathrm{TP}}|)^2}{V_{\mathrm{DD}} - |V_{\mathrm{TP}}| + E_{cp} L_P} = \frac{W_N}{L_N} \frac{\mu_N C_{ox}}{\left(1 + \frac{V_{\mathrm{oL}}}{E_{CN} L_N}\right)} \left((V_{\mathrm{DD}} - V_{\mathrm{TN}}) V_{\mathrm{oL}} - \frac{V_{\mathrm{oL}}^2}{2}\right) \tag{4.21}$$

Simplification as V_{oL} is small :

$$V_{\mathrm{oL}} = \frac{I_{\mathrm{DP}}(\mathrm{sat})}{K_N (V_{\mathrm{DD}} - V_{\mathrm{TN}})}$$

$$K_N = \frac{W_N}{L_N} \mu_N C_{ox}$$

4.7 Sizing Inverters

Problem: Proper selection of W/L values for PU and PD transistor
$\Rightarrow$ Tradeoff between

- timing
- power
- area
- noise margins

For CMOS is the focus on timing, since the inverter

- is ratioless
- and standby power is small

For Pseudo CMOS is the focus on

- noise margin (V_{oL})
- and timing

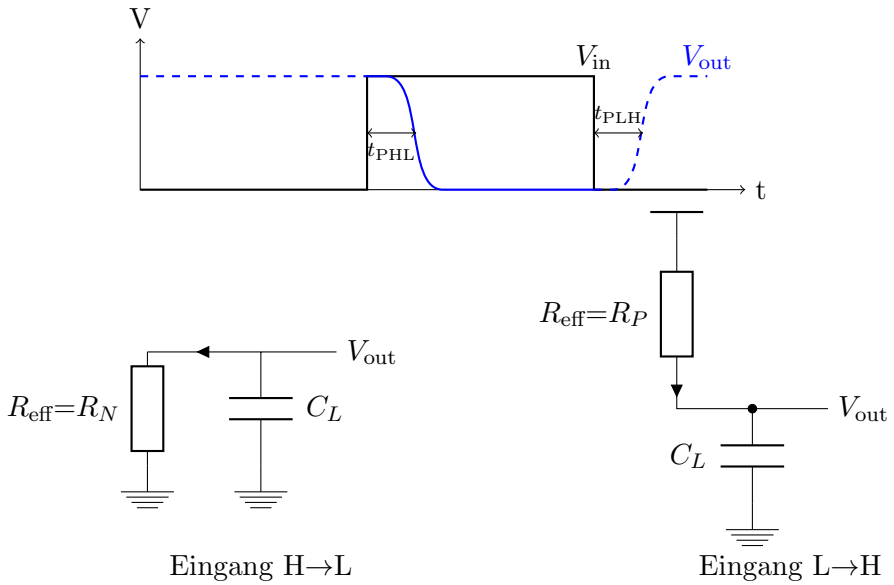


Abb: Simple timing model for inverter sizing

- step input applied
- output propagation time measured at the 50%-point
- inverter modeled with
  - effective on-resistance, R_{eff}
  - driving a load capacitance, C_L

Falling Case:

$$R_{\text{eff}} = R_{\text{N}}$$

$$V_{\text{out}}(t) = V_{\text{DD}} e^{-\frac{t}{R_N C_L}} \tag{4.22a}$$

Rising Case:

$$R_{\text{eff}} = R_{\text{P}}$$

$$V_{\text{out}}(t) = V_{\text{DD}} \left(1 - e^{-\frac{t}{R_P C_L}}\right) \tag{4.22b}$$

In both cases the 50%-point occurs at

$$\tau = 0.69 R_{\text{eff}} C_L \tag{4.22c}$$

For unit-sized devices:

SPICE:

$$R_{\text{eqn}} = 12.5 \frac{k\Omega}{\square} \tag{4.23a}$$

$$R_{\text{eqp}} = 30 \frac{k\Omega}{\square} \tag{4.23b}$$

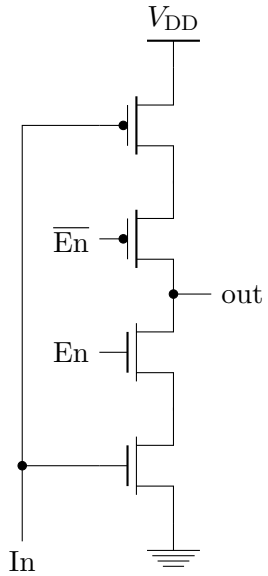
Valid for 0.35μm, 0.18μm and 0.13μm: $\square = \frac{W}{L}$

$$R_N = R_{\text{eqn}} \cdot \frac{L_N}{W_N} \tag{4.24a}$$

$$R_P = R_{\text{eqp}} \cdot \frac{L_P}{W_P} \tag{4.24b}$$

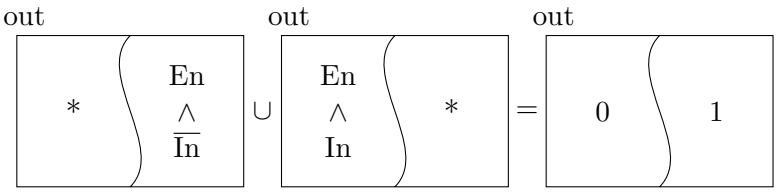
$$\left(\frac{W}{L} = 1\right) \Leftrightarrow (R_N = 12.5k\Omega) \wedge (R_P = 30k\Omega)$$
$$\left(\frac{W}{L} = \frac{1}{2}\right) \Leftrightarrow (R_N = 6.25k\Omega) \wedge (R_P = 15k\Omega)$$

4.8 Tristate Inverters



- High impedance state at the output to effectively disconnect from the bus

In	En	Out
0	0	Z
0	1	1
1	0	Z
1	1	0



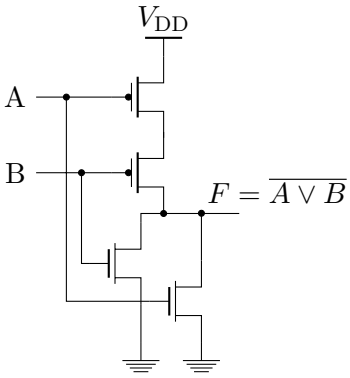
5 Static MOS Gate Circuits

- Content of this chapter:
  Design of combinational and sequential CMOS static logic gates
  - Transistors are seen as logic switches with series resistance
    (unit-sized NMOS: 12.5$k\Omega$ unit-sized PMOS: 30$k\Omega$)
  - Construction of combination logic gates: NAND, NOR, XOR, MUX
    We will examine their:
    - operation

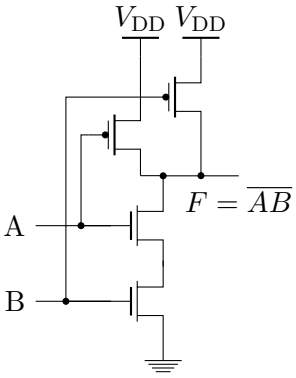
    - VTC
    - transistor sizing
    - 1st order timing characteristics
    - power
  - Construction of sequential logic gates: FlipFlop, Latch We will examine their:
    - constuction using conventional CMOS or Pseudo-NMOS
    - operation, limits and timing constraints
    - set-up (vorher) and hold (nachher) times for D-type FlipFlops / Latches
- Power & Timing are the main design specifications for digital integrated circuits
  - Usually, one is traded off against the other
    - Reducing circuit activity
    - Reducing switching power (operation voltage)
    - Minimizing glitches[4]
    - Equalizing rise & fall times
    - Reducing Subthreshold leakage
- Design metrics (to compare reduction of power and delay)
  - power-delay-product
    $\Rightarrow$ Comparison of single gate configurations that use the same supply voltage and drive the same load (Vergleich von Gattern)
  - energy-delay-product
    $\Rightarrow$ comparison of two different designs that perform the same function (Vergleich von Designs)

5.1 CMOS Gate Circuits

- NMOS bulks are connected to Gnd
- PMOS bulks are connected to V_{DD}



a) 2-input NOR gate



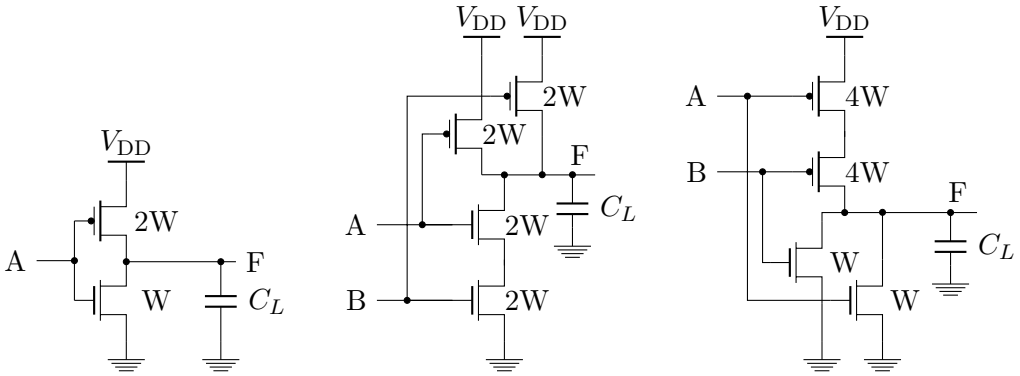
b) 2-input NAND gate

[4] Änderungen einer Schaltung erfolgen nicht gleichzeitig → ungewollte Zustandsänderungen am Ausgang

- Multiple fanin NOR (stack of series-connected PMOS devices)
- Multiple fanin NAND (stack of series-connected NMOS devices)

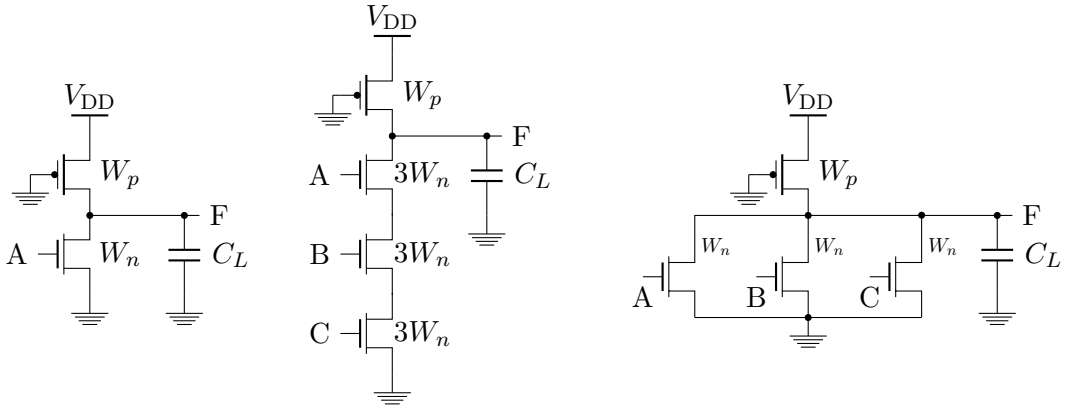
5.2 Basic CMOS Gate Sizing

- Device size controls the rise and fall propagation delays in static CMOS
  $2 : 1 = W_P : W_N$ (as the on-resistance of PMOS is about double that of the NMOS)



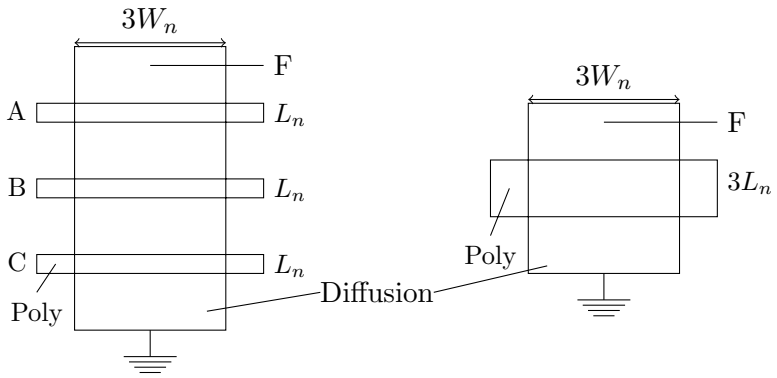
a) INV b) NAND c) NOR

- The ratio of W_n/W_p depends primarily on the desired V_{oL} (for pseudo NMOS inverter)



a) INV b) NAND3 c) NOR3

Layout and equivalent size of 3X device:



Pseudo-NMOS are sized for both V_{oL} and timing when we choose the $\frac{W}{L}$ ratios for the individual devices

$$\frac{1}{W_{eq}} = \frac{1}{W_1} + \frac{1}{W_2} + \frac{1}{W_3} \qquad \text{(5.1, series stack, all devices on)}$$

$$\Rightarrow W_{eq} = \frac{W_1 W_2 W_3}{W_1 W_2 + W_2 W_3 + W_1 W_3}$$

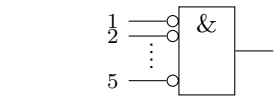
$$W_{eq} = W_1 + W_2 + W_3 \qquad \text{(5.2, parallel stack, all devices on)}$$

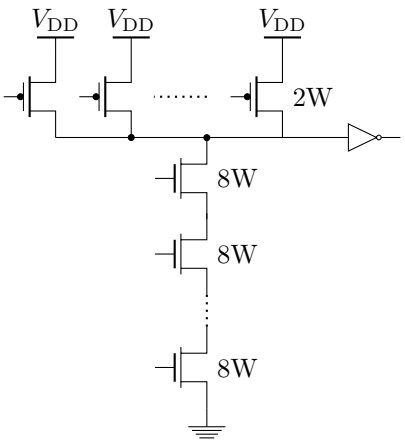
Of course, we design the NOR gate assuming that only one pull-down device is on at a time, since this is the worst case.

5.2.1 Fanin and Fanout Considerations

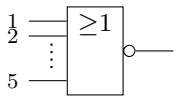
- More than 4 inputs: Resistance of the series stack is too high
- AND8 $\hat{=}$ Pseudo-NMOS NOR8 ($\overline{a} \wedge \overline{b} = \overline{a \vee b}$)
- $\overline{a \wedge b} = \overline{a} \vee \overline{b}$ (NAND8 $\hat{=}$ Pseudo-NMOS NOR8)

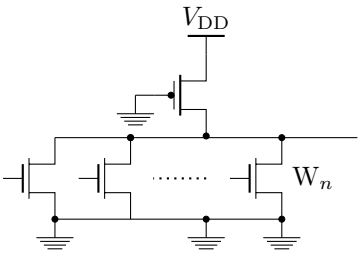
For example:





a) AND8

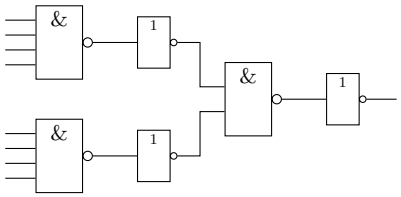




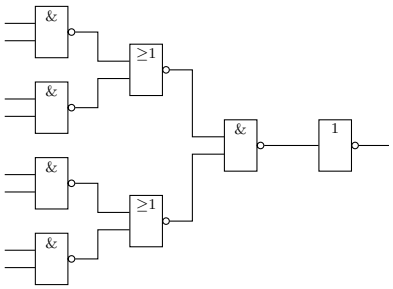
- dissipates more power and exhibits a larger t_{PLH} than static impl
- smaller and t_{PHL} is significantly lower than CMOS impl

b) Pseudo-NMOS NOR8

5.2.2 Multilevel logic implementation (AND8)



c) NAND4 - INV - NAND2 - INV



d) NAND2 - NOR2 - NAND2 - INV

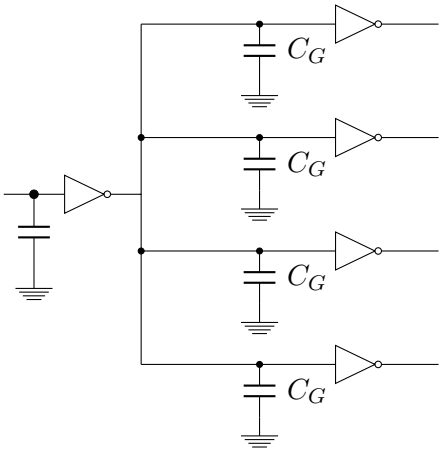


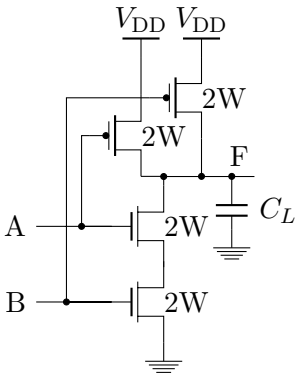
Abb: An inverter driving four identical fanouts FO4 (fanout-of-four)

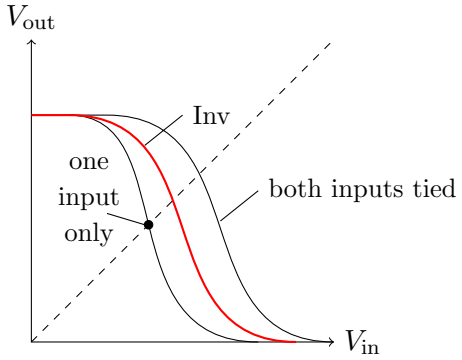
$$\text{fanout ratio} = \frac{\text{total load drivers}}{\text{input cap of driver}} = \frac{4C_G}{C_G}$$

Typically, gates are designed to drive a specific number of fanouts to deliver a specific target delay. Infact, different cells are designed to drive a different number of loads. Ultimately, the choice of the width W is based on this fanout ratio (Chapter 6).

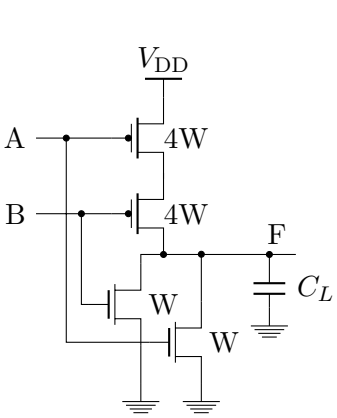
5.2.3 Voltage Transfer Characteristics (VTC) of CMOS gates

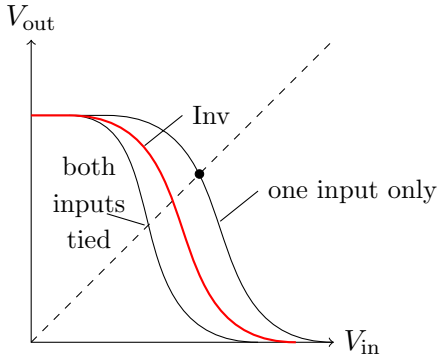
Since there are multiple inputs, the actual characteristics depend on how the inputs are switched.





VTC for NAND2 gate





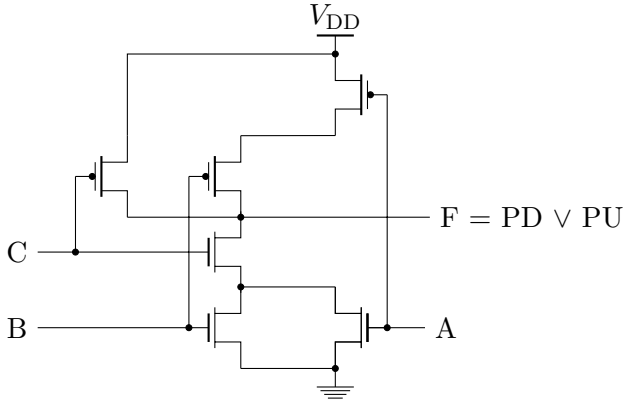
VTC for NOR2 gate

In any case, the single-input switching case is usually taken as the VTC of the multiple input gate.
The NOR has a higher switching threshold than the NAND, and therefore SSNM_L is higher and SSNM_H is lower for the NOR gate as compared to the NAND gate.

5.3 Complex CMOS Gates

- Designing single stage function through the use of complement and duality
- AND-OR-INVERT (AOI) $\rightarrow$ KNF
- OR-AND-INVERT (OAI) $\rightarrow$ DNF
- $\overline{a \wedge b} = \overline{a} \vee \overline{b} \quad (\overline{PD})$
  $a \wedge b = \overline{\overline{a}} \wedge \overline{\overline{b}} \quad (\text{PU})$
  $\Rightarrow$ Dual in der Operation, Komplement in der Aussage

$$
\begin{aligned}
F =& \overline{(A \vee B) \wedge C} = \overline{A \vee B} \vee \overline{C} = \\
& \overline{A} \wedge \overline{B} \vee \overline{C} =: PU(A,B,C) \quad (OAI) \\
\overline{F} =& (A \vee B) \wedge C =: \overline{PD}(A,B,C) \quad (AOI) \\
F =& \overline{PD} \vee PU
\end{aligned}
$$



Complex CMOS gate implementation of $\overline{(A \vee B) \wedge C}$
PU vs $\overline{PD}$:

- „dual in operation“
- „component-wise complement“

$f = a \wedge b$:

a	b	f	$\bar{f}$	$\overline{PD}$	PD	PU
0	0	0	1	1	0	*
0	1	0	1	1	0	*
1	0	0	1	1	0	*
1	1	1	0	*	*	1

Damit:

$f = \text{PD} \vee \text{PU} =$

b \ a	0	0
0	0	*

$\vee$

b \ a	*	*
*	*	1

1. Möglichkeit:

$\overline{PD} \quad \rightarrow \quad f = \overline{a} \vee \overline{b}$

$\overline{PD} = \overline{a} \vee \overline{b} \quad \overline{PD}(\overline{a}, \overline{b})$

$PU = \overline{\overline{a}} \wedge \overline{\overline{b}} \quad PU(\overline{a}, \overline{b})$

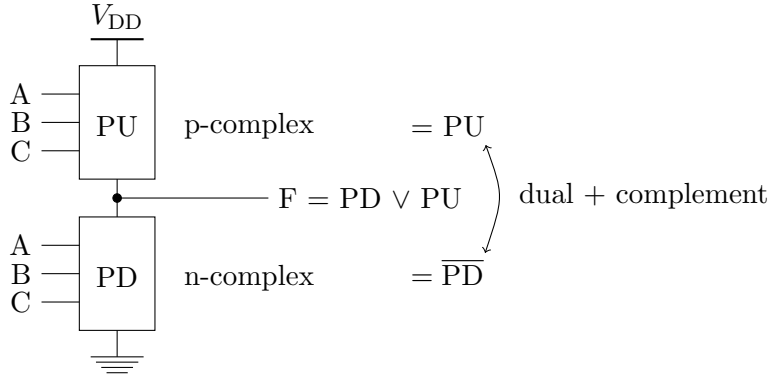
2. Möglichkeit:

$PU \quad \rightarrow \quad \overline{f} = \overline{\overline{a}} \vee \overline{\overline{b}}$

$PU = \overline{\overline{a}} \wedge \overline{\overline{b}} \quad PU(\overline{a}, \overline{b})$

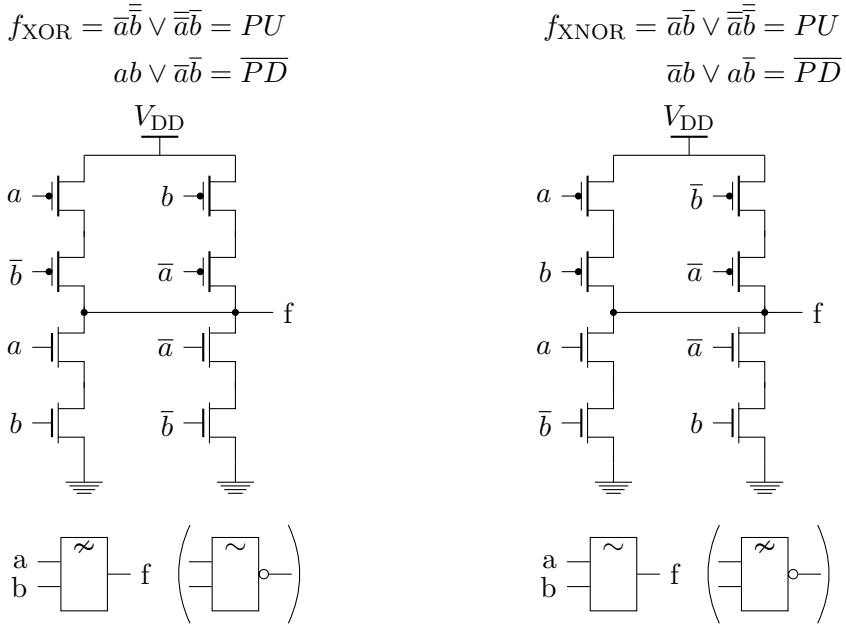
$\overline{PD} = \overline{a} \vee \overline{b} \quad \overline{PD}(\overline{a}, \overline{b})$

$$f = \overline{\overline{a} \vee \overline{b}} \vee (\overline{\overline{a}} \wedge \overline{\overline{b}}) = a \wedge b$$



Generalized complex gate representation

5.4 XOR and XNOR Gates

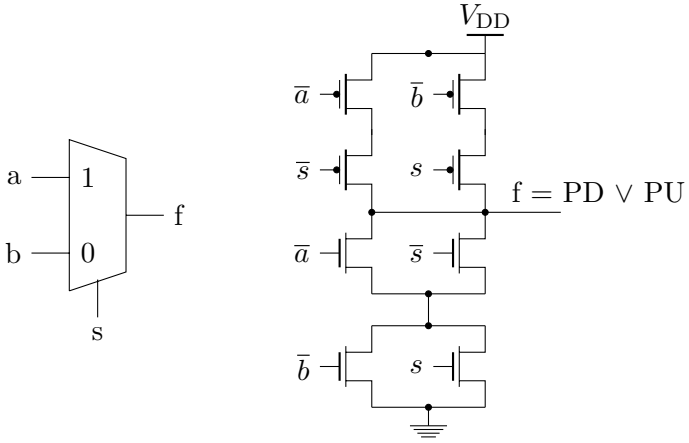


KBS: Signaldarstellung (signal-oriented description)

5.5 Multiplexer Circuits

The multiplexer produces an output by selecting one of N inputs. (KBS: Signaldarstellung)

$$f = \overline{\overline{a}\overline{s}} \wedge \overline{\overline{b}\overline{s}} = \overline{PD}$$



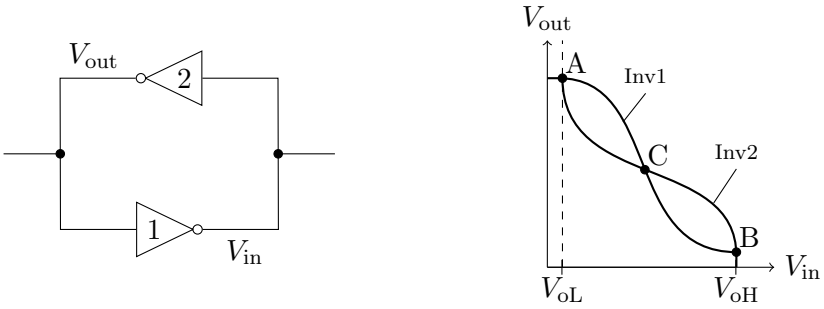
a) logic symbol b) CMOS implementation

5.6 FlipFlops and Latches (sequential circuits)

- feedback loops (history) (positive, regeneration)
  Outputs are dependent on the inputs and the preceding values of outputs (e.g. counters, registers)
- bistable circuit (two stable operating points)
  - Latches, level-sensitive or transparent (e.g. enabled by clock)
  - FF, edge-triggered (discrete point of time)

5.6.1 Basic Bistable Circuits

Cross-coupled inverters and corresponding VTC



- stable operating points: A, B
- instable point (metastable point): C (slope > 1)

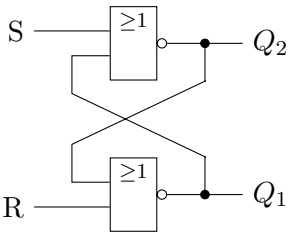
To change stable state:

- trigger voltage pulse
  - sufficient to raise the voltage past V_S
  - $> 2t_p = t_{PHL} + t_{PLH}$

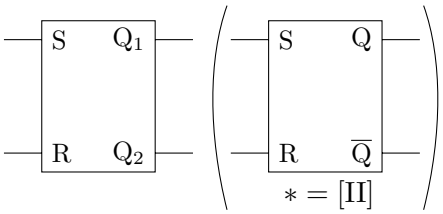
5.6.2 SR Latch (set-reset latch, active high, 2 NORs)

	S	R	Q_1	Q_2
hold	0	0	$\overline{Q_2}$	$\overline{Q_1}$
reset	0	1	0	1
set	1	0	1	0
	1	1	0	0

a) Truth Table



b) circuit



c) symbol (active high inputs)

- S → Q: 2 NOR delays
- S → $\overline{Q}$: 1 NOR delay
- R → Q: 1 NOR delay
- R → $\overline{Q}$: 2 NOR delays

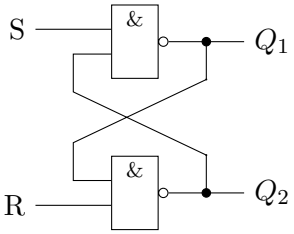
d) Transitions

KBS: Pin-oriented description

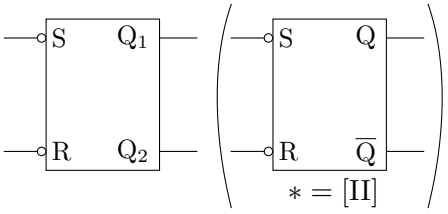
5.6.3 SR Latch (set-reset latch, active low, 2 NANDs)

	S	R	Q_1	Q_2
	0	0	1	1
set	0	1	1	0
reset	1	0	0	1
hold	1	1	$\overline{Q_2}$	$\overline{Q_1}$

a) Truth Table



b) circuit



c) symbol (active low inputs)

- S → Q: 1 NAND delay
- S → $\overline{Q}$: 2 NAND delays
- R → $\overline{Q}$: 2 NAND delays
- R → Q: 1 NAND delay

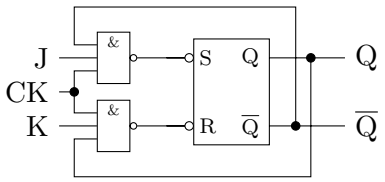
d) Transitions

5.6.4 JK-FlipFlop

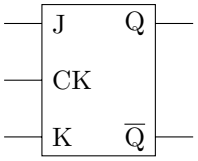
- active high voltage levels
- clocked (not edge-triggered)

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

a) Truth Table



b) circuit

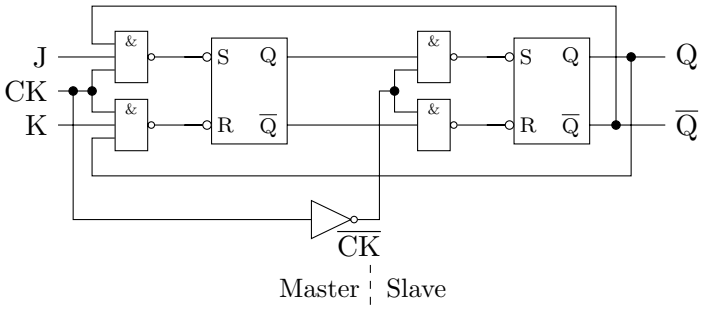


c) symbol

Not to oscillate $\Rightarrow$ very definite restriction on the clock pulse width: $< t_p$

5.6.5 JK Master-Slave FlipFlop

- cascade of two JK FF with the master driving the slave



$t_p > t_p$(Master)

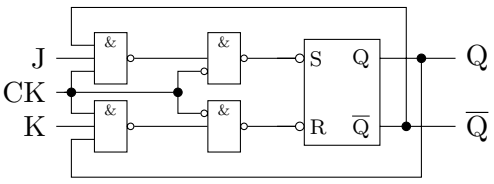
- Slave is a level-sensitive circuit (ones catching)
- any spike or glitch on the J input line will cause the master latch to be set
  $\rightarrow$ Keep 1 state of clock short
  $\rightarrow$ edge-triggered flip-flop

5.6.6 JK Edge-Triggered FlipFlop

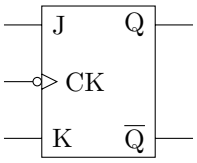
JK negative edge-triggered flip-flop

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

a) Truth Table



b) circuit



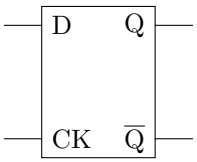
c) symbol

For proper functionality, the values on the J and K inputs must be held stable for a finite length of time before the clock edge (set-up time).
... after the clock edge arrives (hold time, $> 0ns$).
The device usually has additional inputs for direct set and reset so that the outputs can be initialized to the desired settings.

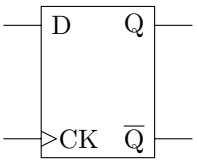
5.7 D Flip-Flop and Latches

D	Q_{n+1}
0	0
1	1

a) truth table



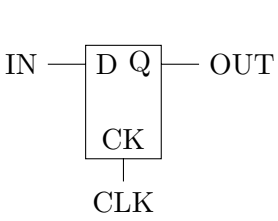
b) transparent

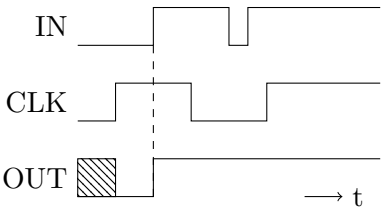


c) edge-triggered

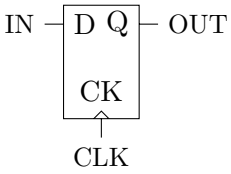
- latch is level-sensitive and transparent
- flip-flop is edge-triggered and otherwise opaque

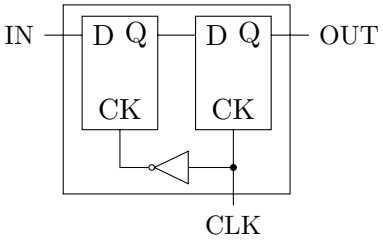
D-Latch operation

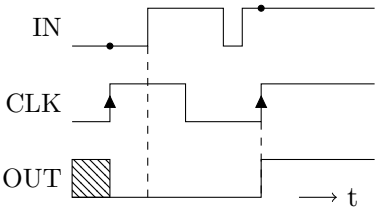




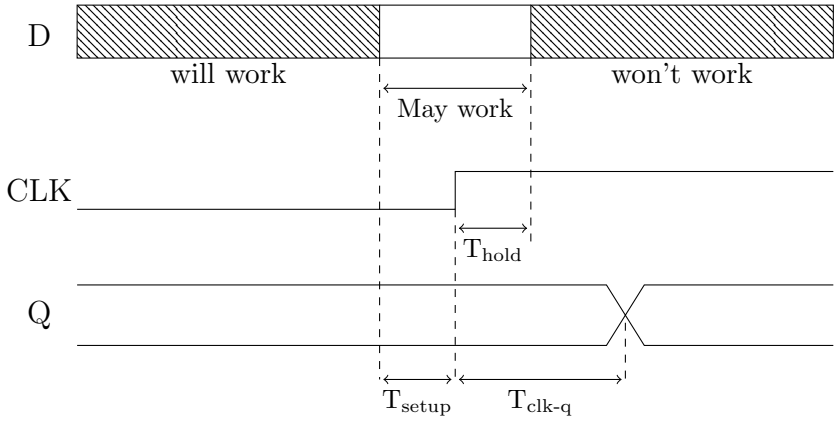
D-Flop operation







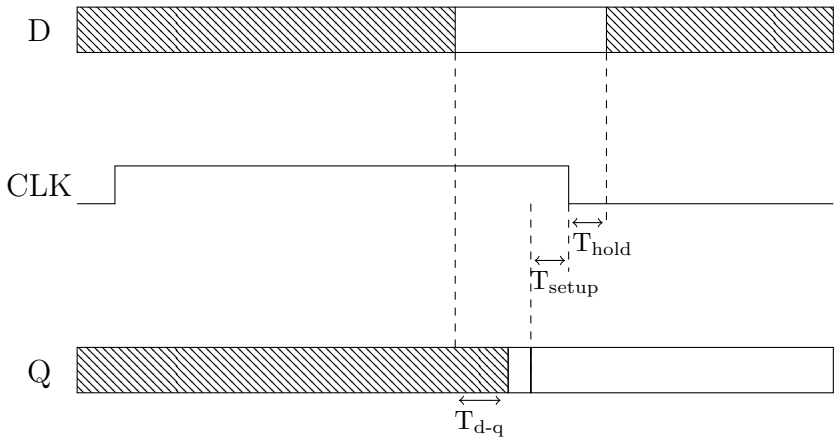
Sample-and-hold circuit: The sampling is done when the clock edge hits the flop.
There are are number of important timing characteristics associated with flops and latches.



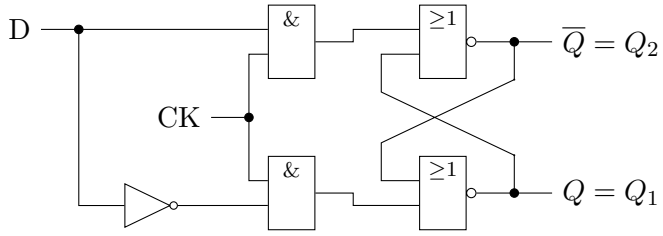
Flip-Flop timing parameters

T_{setup} : The time that the incoming data must be stable before the clock arrives
T_{hold} : The length of time that the data remains stable after the clock arrives for proper operation
uncertainty interval: may work
clock-to-Q delay: $T_{\text{clk-q}}$
overhead: $T_{\text{setup}} + T_{\text{clk-q}}$

When designing flop, we should try to minimize T_{setup}, T_{hold} and $T_{\text{clk-q}}$

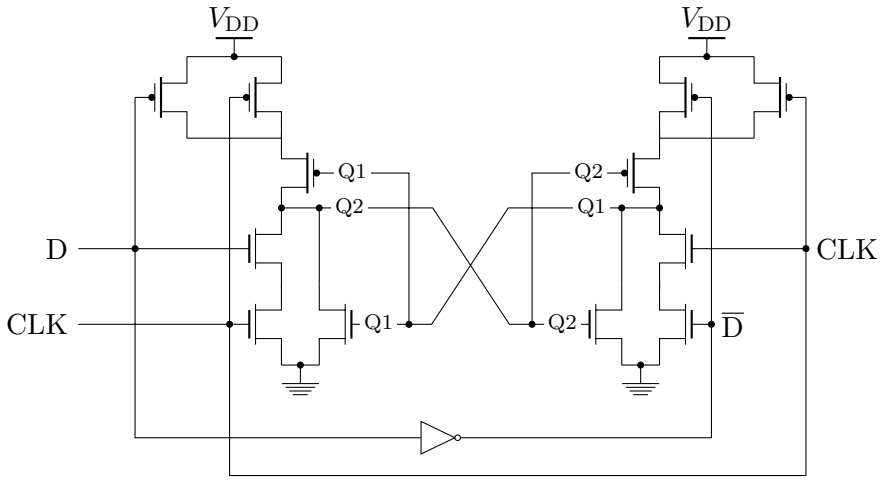


Latch timing parameters
D-to-Q delay: $T_{\text{d-q}}$ (by the latch)



$$Q_2 := \overline{D \wedge CK \vee Q_1} \qquad \overline{PD_2}(D, CK, Q_1) = D \wedge CK \vee Q_1$$
$$PU_2(D, CK, Q_1) = (\overline{D} \vee \overline{CK}) \wedge \overline{Q_1}$$

$$Q_1 := \overline{\overline{D} \wedge CK \vee Q_2} \qquad \overline{PD_1}(\overline{D}, CK, Q_2) = \overline{D} \wedge CK \vee Q_2$$
$$PU_1(\overline{D}, CK, Q_2) = (\overline{\overline{D}} \vee \overline{CK}) \wedge \overline{Q_2}$$



AOI implementation of D-latch

5.8 Power Dissipation in CMOS Gates

- Most important design specification since it affects
  - power grid design
  - chip temperature
  - packaging decisions
  - long-term reliability
- Memory consumes less power than logic circuits
- Timing can control power (tradeoff)

- Power is due to current flowing from the supply to ground
  → add up all sources of current flow from V_{DD} to Gnd and multiply it by the potential difference between the two supply rails

$P = I_{\mathrm{d}} \cdot V_{\mathrm{DD}}$

- Dynamic Power due to
  - capacitance switching
  - short-circuit power due to „crowbar“ current during switching (V_{DD} - Gnd)
  - glitches in the output waveforms
- Static Power due to
  - leakage currents (subthreshold, junction reverse-bias current)
  - dc standby current (e.g. Pseudo-NMOS)

5.8.1 Dynamic (Switching) Power

Charging and Discharging of capacitances: ⇒ current flowing from V_{DD} to Gnd on different parts of the cycle → depending on Frequency f

$$I_{\mathrm{D,\ avg}} = C\frac{dV}{dt} = \frac{C_{\mathrm{L}}\Delta V_{\mathrm{swing}}}{\Delta t} = C_{\mathrm{L}} V_{\mathrm{DD}} f_{\mathrm{avg}} \tag{5.8}$$

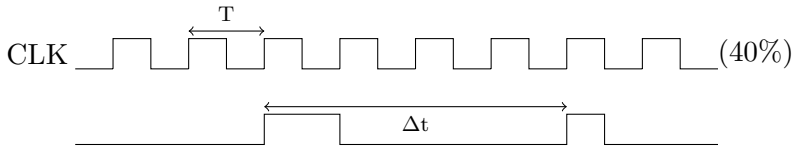
$$P_{\mathrm{switching}} = I_{\mathrm{D,avg}} \cdot V_{\mathrm{DD}} = C_{\mathrm{L}}\Delta V_{\mathrm{swing}} f_{\mathrm{avg}} V_{\mathrm{DD}} = C_{\mathrm{L}} V_{\mathrm{DD}}^2 f_{\mathrm{avg}} \tag{5.9}$$

⇒ Keep C_{L} small
⇒ Reduce the swing (V_{DD})
⇒ Reduce the switching frequency f_{avg}

The approach used to reduce power will be dependent on the design style used:

- timing constrains
- area constraints
- and other tradeoffs

f_{avg} :

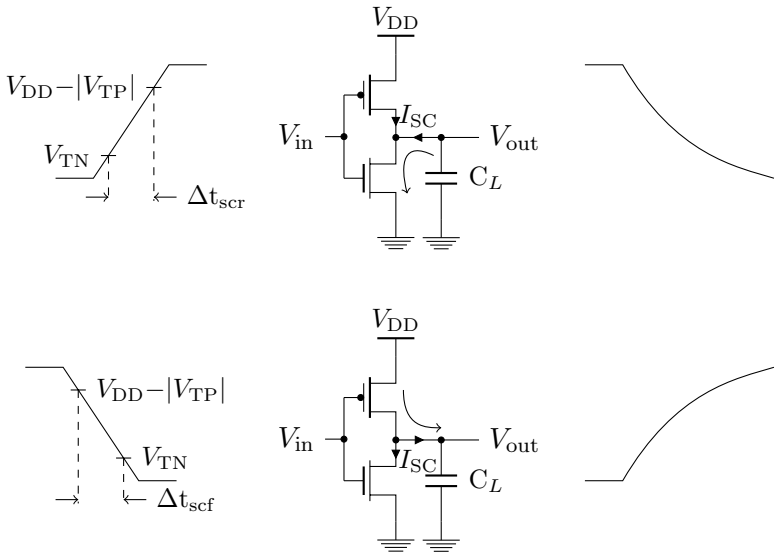


We need two toggles to have power dissipation activity factor $\alpha_{0\mapsto1}$

$$P_{\mathrm{switching}} = \alpha_{0\mapsto1} C_{\mathrm{L}} V_{\mathrm{DD}}^2 f_{\mathrm{CLK}} \qquad \alpha_{0\mapsto1} = \frac{\#\text{toggles}/2}{\#\text{clock cycles}} \tag{5.10}$$

„crowbar“current: $|V_{GS}| > |V_T|$, $V_{TN} < V_{in} < V_{DD} - |V_{TP}|$

$\Delta t_{sc} = \Delta t_{scr} + \Delta t_{scf}$



Short-circuit current flow during switching process

$$
\begin{aligned}
P_{sc} &= I_{sc} \cdot V_{DD} \\
&= \frac{\Delta t_{sc}}{T} \cdot I_{sc,\,avg} \cdot V_{DD} \\
&= \Delta t_{sc} I_{sc,\,avg} V_{DD} f_{avg} \qquad (I\Delta t = C\Delta V) \qquad (5.11) \\
&= C_{sc} V_{DD}^2 f_{CLK} \qquad (C_{sc} = \alpha_{sc} C_L) \\
&= \alpha_{sc} C_L V_{DD}^2 f_{CLK} \qquad (5.12)
\end{aligned}
$$

$$
\begin{aligned}
P_{dynamic} &= P_{switching} + P_{sc} \\
&= \alpha C_L V_{DD}^2 f_{CLK} \qquad (5.13) \\
\alpha &= \underbrace{\alpha_{0\mapsto 1}}_{\text{activity factor}} + \underbrace{\alpha_{sc}}_{\substack{\text{short circuit} \\ \text{current effects}}}
\end{aligned}
$$

In effect, there is a tradeoff between dynamic power of the previous gate and short-circuit power on the next gate.
⇒ input and output edge rates sharp and about equal

Glitches tend to propagate through the fanout gates and cause unintended transisitons in subsequent stages, increasing the power dissipation even further.

⇒ Signals should be made to arrive at roughly the same time at all gate inputs
Keep things balances (glitch free) (path vs gate delay)

5.8.2 Static (standby) Power

(low-power battery-operated or portable devices)

- Leakage currents are beginning to control design decisions

$$I_{\text{sub}} = I_{\text{s}} e^{\frac{q(V_{\text{GS}} - V_{\text{T}} - V_{\text{offset}})}{nkT}} \cdot \left(1 - e^{\frac{-qV_{\text{DS}}}{kT}}\right)$$

  - $V_{\text{GS}} = 0$: under control of V_{T}
  - $V_{\text{DS}} \downarrow$: series transistors to the PU and PD path
    ⇒ Source degeneration
  - $T \downarrow$
- reverse-bias junction currents

$$I_{\text{pn}} = I_0(e^{(q/kT)V_{\text{SB}}} - 1)$$
$$I_0 = A \cdot J_s = -AJ_s$$

  A: Area of Junctions
  J_s: current density
  (bottom of the junction, channel-facing sidewall, pA-nA range)

$$I_{\text{leak}} = I_{\text{sub}} + I_{\text{pn}} \tag{5.14}$$
$$P_{\text{static}} = (I_{\text{sub}} + I_{\text{pn}})V_{\text{DD}} \tag{5.15}$$
$$P_{\text{DC}} = I_{\text{DC}}V_{\text{DD}} \qquad \text{(Pseudo-NMOS)} \tag{5.16}$$

5.8.3 Complete Power Equation

$$P = \alpha C V_{\text{DD}}^2 f_{\text{CLK}} + I_{\text{leak}} V_{\text{DD}} \tag{5.17, CMOS}$$

α : short-circuit current effects included

$$P = \alpha C V_{\text{DD}}^2 f_{\text{CLK}} + I_{\text{leak}} V_{\text{DD}} + \frac{I_{\text{DC}} V_{\text{DD}}}{2} \tag{5.18, Pseudo-NMOS}$$

Geteilt durch 2: dc current flowing half the time

5.9 Power and Delay Tradeoffs

- equalizing the input arrival times will reduce glitches
- equalizing the edge rates will minimize short-circuit currents

Power-delay-product (PDP)

$$\begin{aligned} \text{PDP} &= P_{\text{avg}} \cdot t_p \qquad \left(2t_p = \frac{1}{f}\right) && (5.19) \\ &= CV_{\text{DD}}^2 f \cdot \frac{1}{2f} \\ &= \frac{CV_{\text{DD}}^2}{2} && (5.20) \end{aligned}$$

(energy to perform a specific operation - per toggle -)

$$\begin{aligned} E_C &= \int_0^\infty i_c(t) v_{\text{out}}(t) \mathrm{d}t \\ &= \int_0^\infty C \frac{\mathrm{d}v_{\text{out}}}{\mathrm{d}t} v_{\text{out}}(t) \mathrm{d}t \\ &= \int_0^\infty C v_{\text{out}}(t) \mathrm{d}v_{\text{out}} \\ &= \frac{1}{2} C V_{\text{DD}}^2 \end{aligned}$$

Limitations:

$$\begin{aligned} V_{\text{DD}} \downarrow &\Rightarrow t_p \downarrow \\ C \downarrow &\Rightarrow t_p \downarrow \end{aligned}$$

Energy-Delay-Product

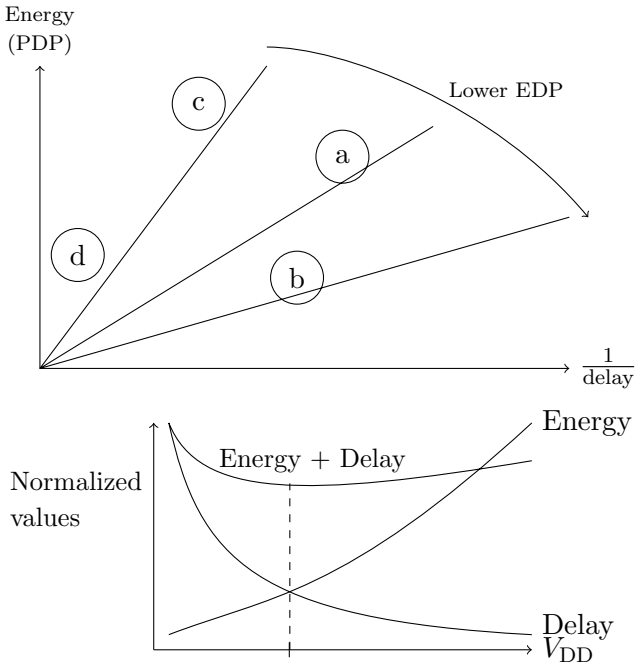
$$EDP = PDP \cdot t_p \tag{5.21}$$

New formulation for tp:

$$\begin{aligned} I &= C\frac{dV}{dt} \\ \Delta t &= C\frac{\Delta V}{I} \\ t_p &= \frac{C\Delta V}{I_{\text{sat}}} \approx \frac{CV_{\text{DD}}}{K_2(V_{\text{DD}} - V_{\text{T}})} \end{aligned} \tag{5.22}$$

K_2: constant that depends on device sizes

$$\text{EDP} = \frac{C^2 V_{\text{DD}}^3}{2K_2(V_{\text{DD}} - V_{\text{T}})} \tag{5.23}$$



optimum EDP:

$$\frac{\Delta \text{EDP}}{\Delta V_{\text{DD}}} = 0$$

$$V_{\text{DD}}^* = \frac{3}{2} V_{\text{T}}$$

Used to set the supply voltage for a given technology, at least!

5.10 Summary

For a series stack with three devices, the width of a single equivalent device is

$$W_{eq} = \frac{W_1 W_2 W_3}{W_1 W_2 + W_2 W_3 + W_1 W_3} \qquad \text{(series stack)}$$

For a parallel set of devices, the equiavalent width with all devices turned on is

$$W_{eq} = W_1 + W_2 + W_3 \qquad \text{(parallel devices)}$$

Average propagation delay

$$t_p = \frac{t_{\text{PHL}} + t_{\text{PLH}}}{2}$$

Dynamic and static power

$$P_{\text{dynamic}} = \alpha C_{\text{L}} V_{\text{DD}}^2 f_{\text{CLK}}$$
$$P_{\text{static}} = (I_{\text{sub}} + I_{\text{pn}}) V_{\text{DD}}$$

For a standard CMOS gate, the complete power equation is given by

$$P = \alpha C V_{\text{DD}}^2 f_{\text{CLK}} + I_{\text{leak}} V_{\text{DD}}$$

For a pseudo-NMOS gate, the complete power equation is given by

$$P = \alpha C V_{\text{DD}}^2 f_{\text{CLK}} + I_{\text{leak}} V_{\text{DD}} + \frac{I_{\text{DC}} V_{\text{DD}}}{2}$$

Energy-Delay-Product:

$$\text{EDP} = \text{PDP} \cdot t_p = P \cdot t_p \cdot t_p = \frac{C^2 V_{\text{DD}}^3}{2K_2(V_{\text{DD}} - V_{\text{T}})}$$

6 High-Speed CMOS Logic Design

- to perform the desired function
- to satisfy the timing requirements

which means:

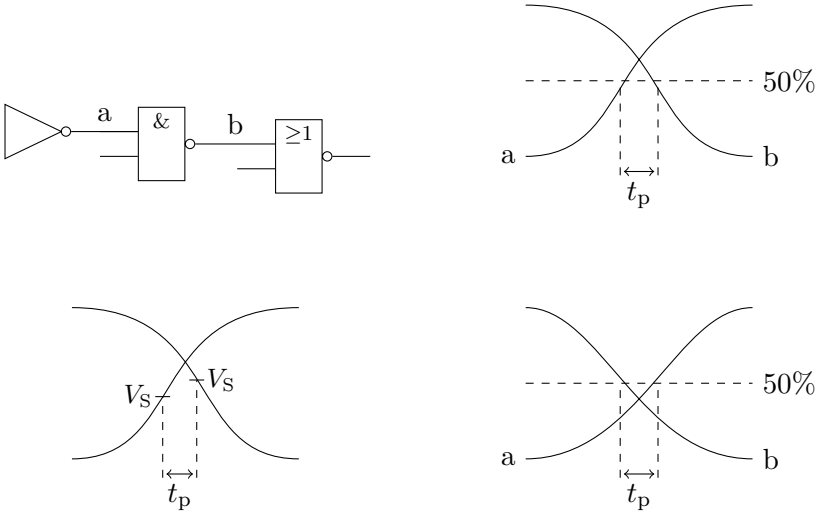
- proper selection of logic gates
- proper gate sizing

critical path:

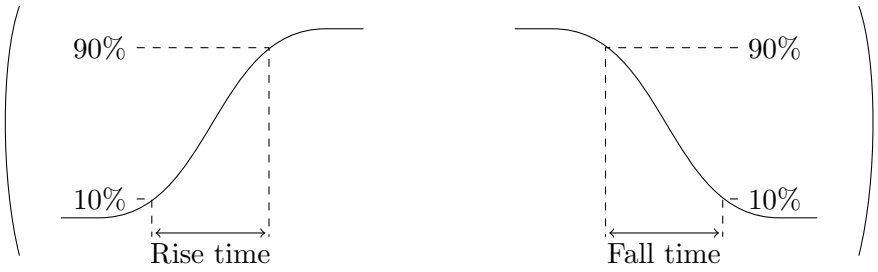
- worst case delay
  - driving resistance
  - load capacitance

„back-of-the-envelope “ hand calculations:

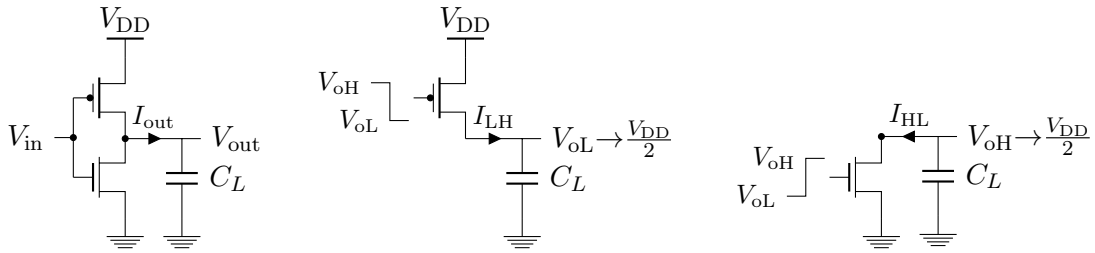
- step function (ramp function)
- propagation delay definitions



Negative delay indicates a slow gate in the path
50% definition is the most practical and intuitive reference point for propagation delay



6.1 Switching Time Analysis



a) b) t_{PHL} c) t_{PLH}

$$I = C_{\mathrm{L}} \frac{\mathrm{d}V}{\mathrm{d}t}$$
$$\Delta t \approx C_{\mathrm{L}} \frac{\Delta v}{I_{\mathrm{DS}}}$$
$$t_{\mathrm{PLH}} = \frac{C_{\mathrm{L}} V_{\mathrm{DD}}/2}{I_{\mathrm{LH}}}$$
$$t_{\mathrm{PHL}} = \frac{C_{\mathrm{L}} V_{\mathrm{DD}}/2}{I_{\mathrm{HL}}}$$

Average propagation delay:

$$t_{\mathrm{p}} = \frac{t_{\mathrm{PLH}} + t_{\mathrm{PHL}}}{2}$$

$\underline{0.13\mu m}$

$$V_{\mathrm{Dsat}} = \frac{V_{\mathrm{GS}} - V_{\mathrm{T}})E_C L}{(V_{\mathrm{GS}} - V_{\mathrm{T}}) + E_C L} = \frac{(1.2 - 0.4)0.6}{(1.2 - 0.4) + 0.6} = 0.34V \text{ (NMOS)}$$

$V_{\mathrm{DS}} \in [1.2; 0.6]V \Rightarrow V_{\mathrm{DS}} > V_{\mathrm{Dsat}} \Rightarrow$ saturation of NMOS

$$t_{\mathrm{PHL}} = \frac{C_{\mathrm{L}} V_{\mathrm{DD}}/2}{I_{\mathrm{Dsat,n}}} = 0.7 R_{\mathrm{N}} C_{\mathrm{L}}$$
$$R_{\mathrm{N}} = \frac{V_{\mathrm{DD}}/2}{0.7 I_{\mathrm{Dsat,n}}} \tag{6.4b}$$

$$V_{\mathrm{Dsat}} = \frac{(1.2 - 0.4)2.4}{(1.2 - 0.4) + 2.4} = 0.6V \text{ (PMOS)}$$

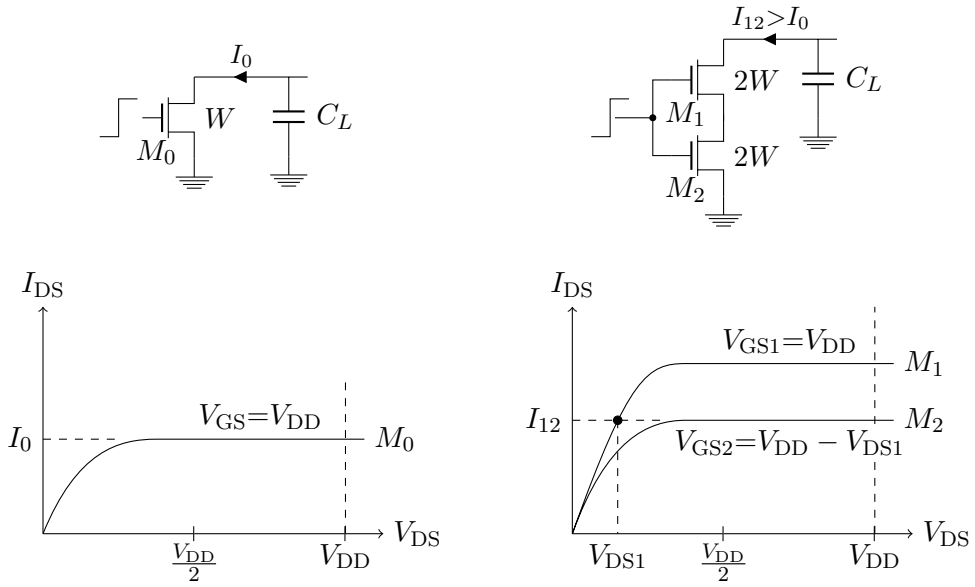
$V_{\mathrm{SD}} \in [1.2; 0.6]V \Rightarrow V_{\mathrm{SD}} > V_{\mathrm{Dsat}} \Rightarrow$ saturation of PMOS

$$t_{\mathrm{PHL}} = \frac{C_{\mathrm{L}} V_{\mathrm{DD}}/2}{I_{\mathrm{Dsat,p}}} = 0.7 R_{\mathrm{P}} C_{\mathrm{L}}$$
$$R_{\mathrm{P}} = \frac{V_{\mathrm{DD}}/2}{0.7 I_{\mathrm{Dsat,p}}} \tag{6.5b}$$

$$R_{\mathrm{eqn}} = 12.5k\Omega/\square$$
$$R_{\mathrm{N}} = R_{\mathrm{eqn}}(\frac{L}{W})_n$$
$$R_{\mathrm{eqp}} = 30k\Omega/\square$$
$$R_{\mathrm{P}} = R_{\mathrm{eqp}}(\frac{L}{W})_p$$

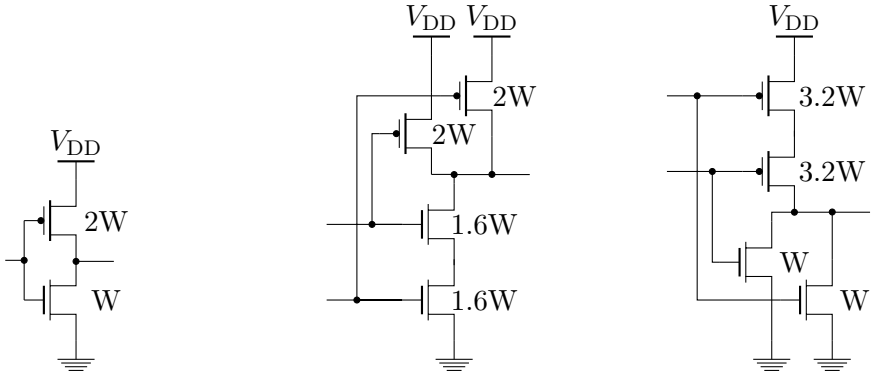
works well for timing calculation in digital, should not be used for any other purpose!
$\Rightarrow$ In reality, the on-resistance is nonlinear and its value depends on the applied voltages.

6.1.1 Gate Sizing Revisited - Velocity Saturation Effects



Stacked devices with velocity saturation (for long channel devices quadratic dependence)

To equalize the delays the stacked devices can be reduced by roughly 20-25%
For a pair of long channel devices in the series stack, the discharge current would actually be lower than the single transistor case (current drops off quadratically)



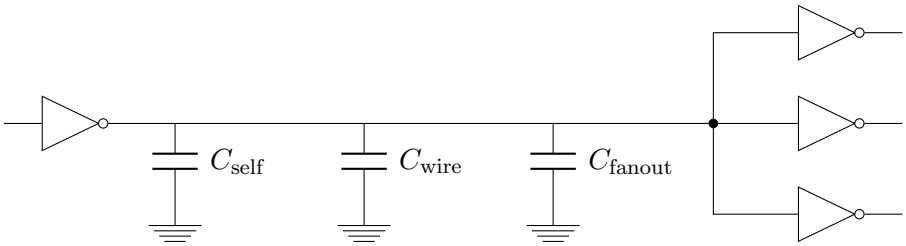
a) INV b) NAND c) NOR

Transistor sizing for NAND and NOR including velocity saturation (Scaled by 0.8)
body effect ⇒ reduce the current of the top device
additional self capacitances
noise margin, rise and fall time
satisfactory to use 2W and 4W

6.2 Detailed Load Capacitance Calculation

- self-loading capacitance
- interconnect (or wire) capacitance
- fanout capacitance

Lumped capacitance: $C_{\text{load}} = C_{\text{self}} + C_{\text{wire}} + C_{\text{fanout}}$



Components of the loading capacitance on a gate

6.2.1 Fanout Gate Capacitance

$$C_{\text{fanout}} = \sum C_{\text{G}}$$

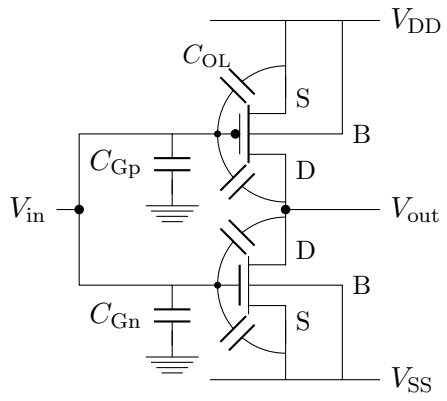
$$\begin{aligned} C_{\text{G}} &= C_{\text{Gn}} + 2C_{\text{OL}} + C_{\text{Gp}} + 2C_{\text{OL}} \\ &= C_{\text{ox}}LW_n + 2C_{\text{ol}}W_n + C_{\text{ox}}LW_p + 2C_{\text{ol}}W_p \\ &= \underbrace{(C_{\text{ox}}L + 2C_{\text{ol}})}_{C_{\text{g}}}(W_n + W_p) \end{aligned}$$

$$C_{\text{g}} = 1.6 \cdot 10^{-6}\frac{F}{cm^2} \cdot 0.1\mu m + 2(0.25\frac{fF}{\mu m}) = 2\frac{fF}{\mu m}$$

$$C_{\text{G}} = C_{\text{g}}W = 2\frac{fF}{\mu m} \cdot (W_{\text{n}} + W_{\text{p}})$$

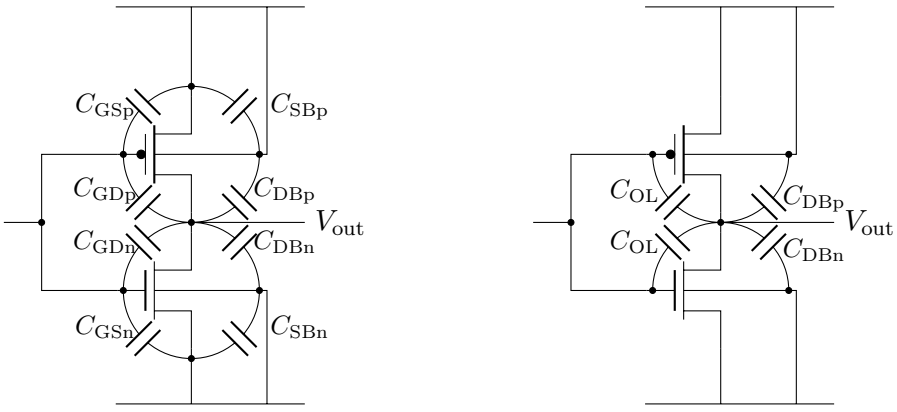
$$C_{\text{fanout}} = \sum C_{\text{G}} = n \cdot C_{\text{G}} = n \cdot \sum C_{\text{g}}W \quad \sum \text{ vs. } n$$

$$\sum C_{\text{G}} = 2\frac{fF}{\mu m} \cdot (\underbrace{W_{\text{p1}} + W_{\text{n1}}}_{\text{1st}} + \underbrace{W_{\text{p2}} + W_{\text{n2}}}_{\text{2nd}} + ...)$$



6.2.2 Self-Capacitance Calculation

The self-capacitance is the sum of the capacitances connected to the output, V_{out}



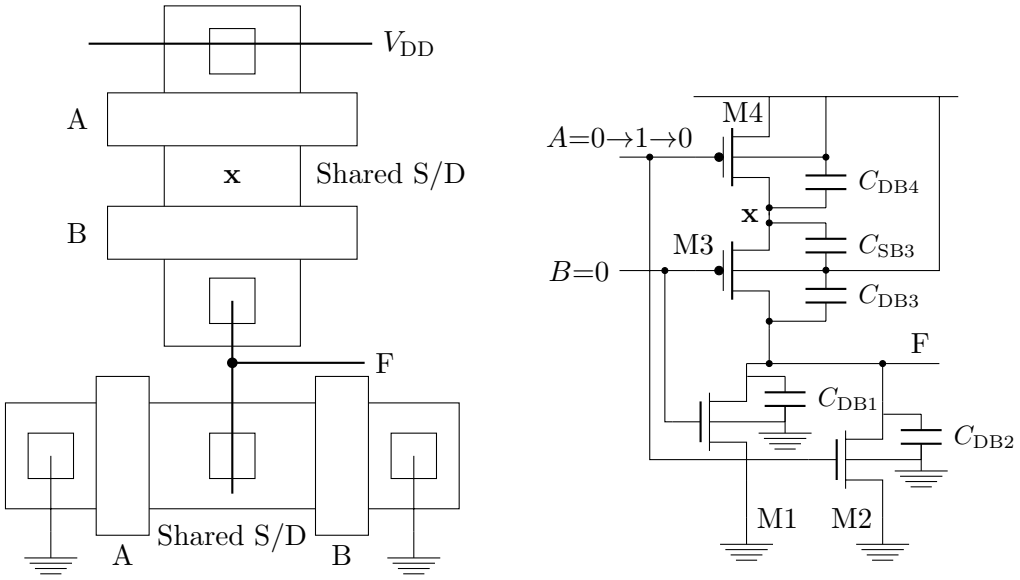
Output Capacitance calculation

The transistors are in saturation or cutoff.

Miller effect modeling

The overlap capacitance experiences a voltage swing of $2V_{DD} \Rightarrow 2C_{OL}$

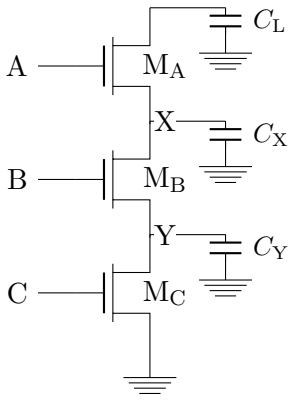
$$
\begin{aligned}
C_{\text{self}} &= C_{\text{DBn}} + C_{\text{DBp}} + 2C_{\text{OL}} + 2C_{\text{OL}} \\
&= C_{\text{jn}}W_n + C_{\text{jp}}W_p + 2C_{\text{ox}}(W_{\text{n}} + W_{\text{p}}) \\
&= C_{\text{eff}}(W_{\text{n}} + W_{\text{p}}) \\
C_{\text{eff}} &= C_{\text{j}} + 2C_{\text{ol}} \approx 0.5\frac{fF}{\mu m} + 2(0.25)\frac{fF}{\mu m} = 1\frac{fF}{\mu m}
\end{aligned}
$$



Self-capacitances for a NOR gate

$$
\begin{aligned}
t_{\text{PHL}} : C_{\text{self}} &= C_{\text{DB1}} + C_{\text{DB2}} + C_{\text{DB3}} + \frac{2}{3}\left(C_{\text{SB3}} + C_{\text{DB4}}\right) \\
&= C_{\text{DB12}} + C_{\text{DB3}} + \frac{2}{3}C_{\text{SDB34}}
\end{aligned}
\tag{6.11}
$$

„Do not double count shared regions!“
The actual delay depends on the order in which inputs switch.



Propagation delay depends on

arrival of A, B and C.

A $\mapsto$ B $\mapsto$ C	all capacitances (C_L+C_x+C_y) must be discharged
C $\mapsto$ B $\mapsto$ A	only C_L must be discharged

In a series stack, the delay increases as the late arriving input is further from the output.

Late arriving signal is C: $C_\mathrm{L} + C_\mathrm{x} + C_\mathrm{y}$
B: $C_\mathrm{L} + C_\mathrm{x}$
A: C_L

There are a number of ways to design around this delay difference.
For example:
$M_C > M_B > M_A$
The correspondingly larger caps act to offset the advantages of progressive sizing!

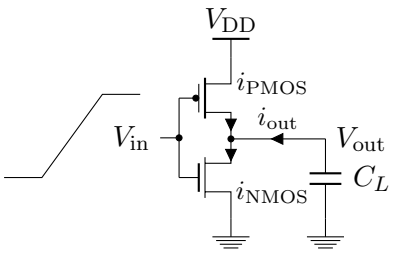
6.2.3 Wire Capacitance

(lumped wire capacitance)

$$C_\mathrm{wire} = C_\mathrm{int} L_w = 0.2 \frac{fF}{\mu m} \cdot \text{wire length}$$

6.3 Improving Delay Calculations with Input Slope

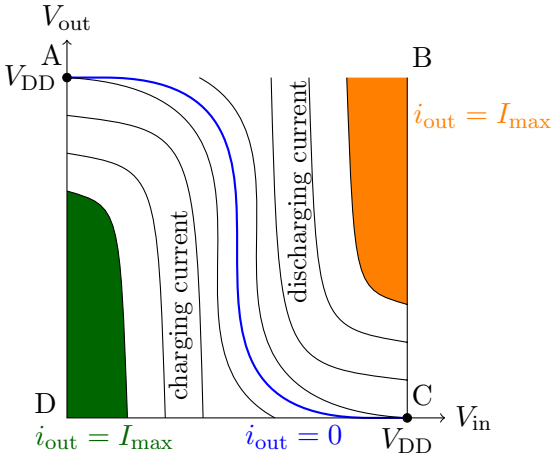
We explore the effect of a finite input slope on the propagation delay



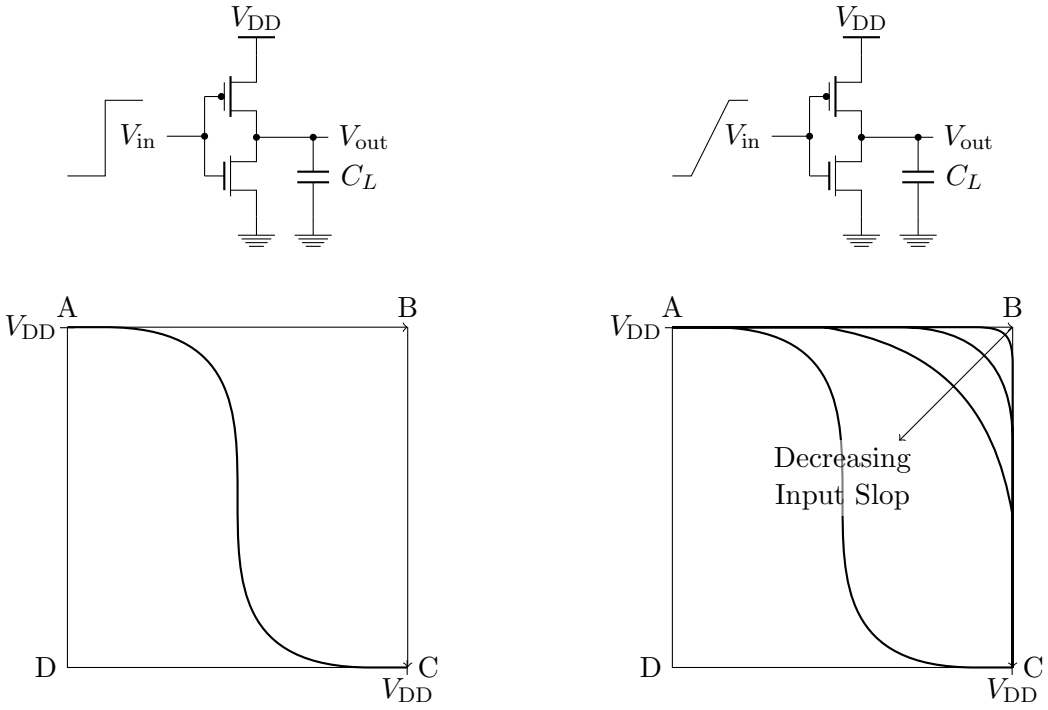
KCL at output

$$I_\mathrm{out} = -C_\mathrm{L} \frac{dV_\mathrm{out}}{dt} = I_\mathrm{NMOS} - I_\mathrm{PMOS}$$

All three currents are a function of V_in and V_out (Großsignalverhalten vs Kleinsignalverhalten, GBS vs KBS)
$\Rightarrow$ contour map



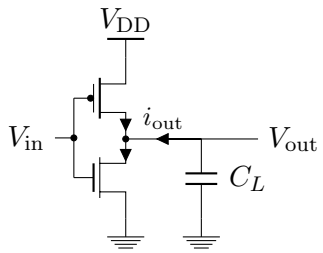
Simplified inverter output current as a function of V_{out} and V_{in}

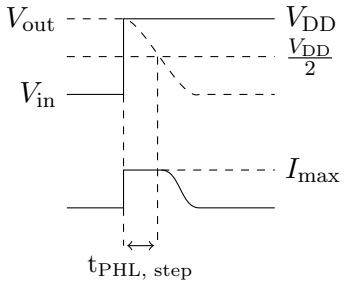


a) Step input trajectory

b) Ramp input trajectory

Example: Delay Calculation with Step Input





$$I_{out} = I_{max} = C_L \frac{dV_{out}}{dt} = C_L \frac{V_{DD}/2}{t_{PHL,\ step}} \Leftrightarrow$$

$$t_{PHL,\ step} = C_L \frac{V_{DD}/2}{I_{max}}$$

Example: Delay Calculation with Ramp Input

$$
\begin{aligned}
I_{\text{out}} &= -C_{\text{L}}\frac{dV_{\text{out}}}{dt} \Leftrightarrow \\
\int I_{\text{out}}dt &= -\int C_{\text{L}}dV_{\text{out}} \\
\int_0^{t_{\text{r}}/2} I_{\max}\frac{t}{t_{\text{r}}/2}dt &+ \int_{t_{\text{r}}/2}^{t_{\text{PHL, ramp}}} I_{\max}dt = C_{\text{L}}\int_0^{V_{\text{DD}}/2} dV_{\text{out}} \\
\frac{I_{\max}}{t_{\text{r}}/2}\frac{t^2}{2}\Big|_0^{t_r/2} &+ I_{\max}t\Big|_{t_{\text{r}}/2}^{t_{\text{PHL, ramp}}} = C_{\text{L}}\frac{V_{\text{DD}}}{2} \\
I_{\max}\frac{t_{\text{r}}}{4} &+ I_{\max}(t_{\text{PHL, ramp}} - t_r/2) = C_{\text{L}}\frac{V_{\text{DD}}}{2}f \\
t_{\text{PHL, ramp}} &= \frac{t_{\text{r}}}{4} + \frac{C_{\text{L}}V_{\text{DD}}/2}{I_{\max}} \\
t_{\text{PHL, ramp}} &= \frac{t_{\text{r}}}{4} + t_{\text{PHL, step}} \quad \text{with } t_{\text{r}} \cong 2t_{\text{PLH, step}} \\
t_{\text{PHL, ramp}} &= \frac{2t_{\text{PLH, step}}}{4} + t_{\text{PHL, step}} \stackrel{!}{=} \frac{2t_{\text{PHL, step}}}{4} + t_{\text{PHL, step}}
\end{aligned}
$$

$$
\begin{aligned}
t_{\text{ramp}} &= \Delta t_{\text{ramp}} + t_{\text{step}} = \frac{t_{\text{in}}}{2} + t_{\text{step}} \\
\text{mit } t_{\text{in}} &= 0.7RC\frac{1}{2} \approx 0.3RC \\
t_{\text{step}} &= 0.7RC \\
&\Rightarrow t_{\text{ramp}} \approx RC
\end{aligned}
$$

$$\boxed{\text{total\_delay} \approx \sum_i R_{\text{i}}C_{\text{i}}}$$

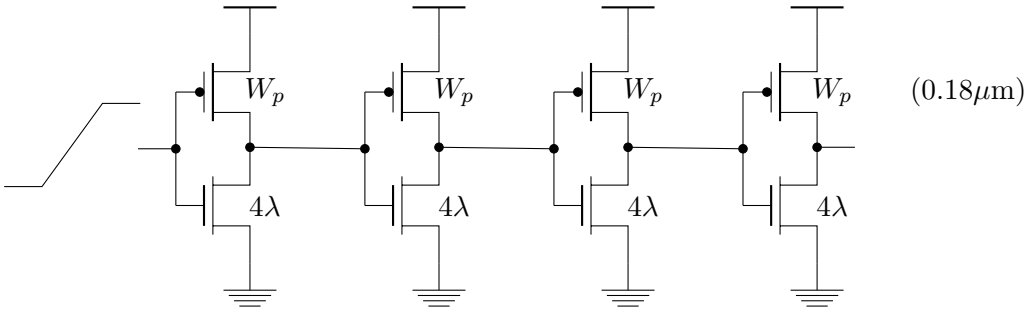
$\sum \gg$ Product of on-resistance and load capacitance $\ll$

Example 6.7 Optimal PMOS Device Size For Inverter Chain

Inverter sizing can be performed

a) to equalize rise/fall delays or

b) to minimize the propagation delay



a)

$$\frac{R_{\text{effp}}}{R_{\text{effn}}} = \frac{30k\Omega}{12.5k\Omega} = 2.4 \Leftrightarrow \frac{W_P}{W_N} = 2.4$$

$$W_P = 2.4 \cdot 4\lambda \approx 10\lambda \quad (0.18\mu m, \lambda = 100nm)$$

$$C_{\text{eff}} = 1\frac{fF}{\mu m} \qquad C_{\text{self}} = C_{\text{eff}}\,(W_N + W_P) = 1.4fF$$

$$C_{\text{g}} = 2\frac{fF}{\mu m} \qquad C_{\text{fanout}} = C_{\text{g}}\,(W_N + W_P) = 2.8fF$$

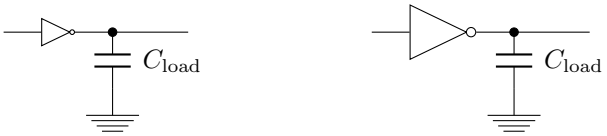
delay of the chain

$$\tau_{\text{total}} = 4t_{\text{PHL}} = 4R_{\text{eff}}C_{\text{load}} = 4(12.5k\Omega)\frac{2\lambda}{4\lambda}4.2fF = 105ps$$

b) page 275: $\tau_{\text{total}} = 97.6ps$

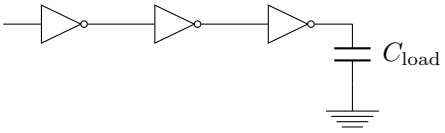
Designers typically use a 2:1 ratio since it is a reasonable compromise between minimum delay and equal rise/fall times.

6.4 Gate Sizing for Optimal Path Delay

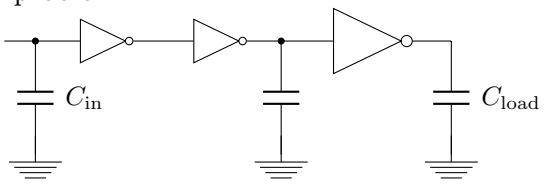


a) b)

Sizing inverters to drive a large capacitive load



Optimal path delay problem



Input loading effects of large drivers

The proper specification of the optimal path delay problem involves the minimization of the path delay given **both input and output** loading constraints.

$$\text{path\_delay} = \sum R_i C_i$$

R_i: driver resistance of gate i
C_i: output loading capacitance on the gate i

6.5 Inverter Chain Delay Optimization - FO4 Delay

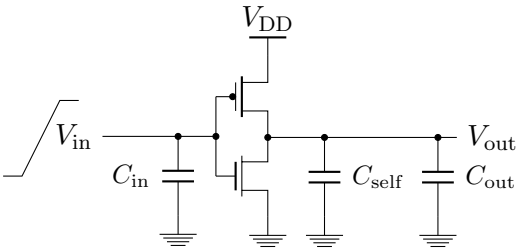
inverter size $\uparrow \Rightarrow$ delay $\downarrow \wedge C_{\text{G}} \uparrow$

$$C_{\text{in}} = C_{\text{G}}(W_n + W_p) = C_{\text{G}}(W_n + 2W_n) = C_{\text{G}} 3W_n$$
$$R_{\text{eff}} = R_{\text{eqn}} \left(\frac{L_n}{W_n} \right)$$

intrinsic property of the gate

$$C_{\text{inv}} = R_{\text{eff}} C_{\text{in}} = R_{\text{eqn}} \frac{L_{\text{n}}}{W_{\text{n}}} C_{\text{g}} 3W_{\text{n}} = 3R_{\text{eqn}} C_{\text{g}} L_{\text{n}}$$

We want to know how effective a gate is at driving a load capacitance while minimizing its input capacitance.
The self-capacitance term is not part of the intrinsic time constant.



Delay for inverter driving a load

$$\begin{aligned} t_{\text{delay}} &= R_{\text{eff}}(C_{\text{out}} + C_{\text{self}}) \\ &= R_{\text{eff}}C_{\text{in}}\left(\frac{C_{\text{out}}}{C_{\text{in}}} + \frac{C_{\text{self}}}{C_{\text{in}}}\right) \\ &= \tau_{\text{inv}}\left(\frac{C_{\text{out}}}{C_{\text{in}}} + \gamma_{\text{inv}}\right) \end{aligned}$$

$$\boxed{\gamma_{\text{inv}} = \frac{C_{\text{self}}}{C_{\text{in}}}}$$

$$\boxed{\text{fanout ratio (electrical effort): } f = \frac{C_{\text{out}}}{C_{\text{in}}}}$$

$\underline{0.13\mu m}$:

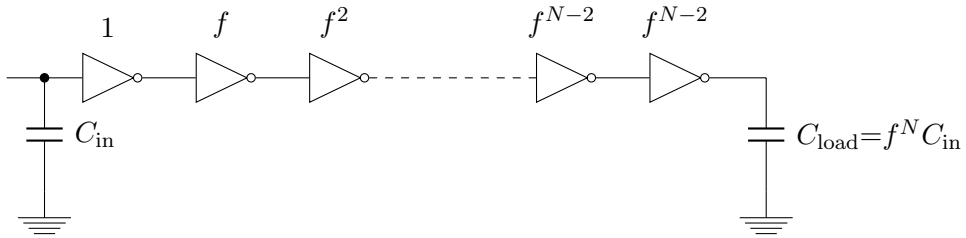
$$\tau_{\text{inv}} = 3R_{\text{eqn}}C_{\text{g}}L_{\text{n}} = 3 \cdot 12.5k\Omega \cdot \frac{fF}{\mu m} \cdot 0.1\mu m = 7.5ps$$
$$\gamma_{\text{inv}} = \frac{C_{\text{self}}}{C_{\text{in}}} = \frac{C_{\text{eff}}3W}{C_{\text{g}}3W} = \frac{1fF/\mu m}{2fF/\mu m} = 0.5$$

$\underline{0.18\mu m}$:

$$\tau_{\text{inv}} = 15ps$$
$$\gamma_{\text{inv}} = 0.5$$

$$\begin{aligned} \text{total\_delay} &= \sum_{j=1}^{N} \tau_{\text{inv}}\left(\frac{C_{\text{j+1}}}{C_{\text{j}}} + \gamma_{\text{inv}}\right) \\ &= \sum_{j} \tau_{\text{inv}}\left(\frac{W_{\text{j+1}}}{W_{\text{j}}} + \gamma_{\text{inv}}\right) \end{aligned}$$

$$D_j = \tau_{\text{inv}}\left(\frac{W_{\text{j}}}{W_{\text{j-1}}} + \gamma_{\text{inv}}\right) + \tau_{\text{inv}}\left(\frac{W_{\text{j+1}}}{W_{\text{j}}} + \gamma_{\text{inv}}\right)$$
$$\frac{\delta D_j}{\delta W_{\text{j}}} = \tau_{\text{inv}}\frac{1}{W_{\text{j1}}} - \tau_{\text{inv}}\frac{W_{\text{j+1}}}{W_{\text{j}}^2} = 0$$
$$W_{\text{j}} = \sqrt{W_{\text{j+1}} \cdot W_{\text{j-1}}}$$



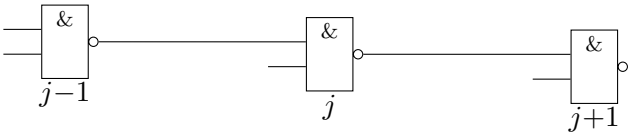
Series chain of inverters

$$f^N C_{\text{in}} = C_{\text{load}} \Rightarrow N = \frac{\ln(C_{\text{load}}/C_{\text{in}})}{\ln(f)} \tag{6.21}$$

$$\begin{aligned} \text{gate\_delay} &= \tau_{\text{inv}} \left(\frac{C_{\text{j}}}{C_{\text{j1}}} + \gamma_{\text{inv}} \right) \\ \text{total\_delay} &= N \cdot \tau_{\text{inv}} \left(\frac{C_{\text{j}}}{C_{\text{j-1}}} + \gamma_{\text{inv}} \right) \qquad (6.22) \\ &= \frac{\ln(C_{\text{load}}/C_{\text{in}})}{\ln(f)} \cdot \tau_{\text{inv}}(f + \gamma_{\text{inv}}) \qquad (6.23) \end{aligned}$$

Optimal value of f lies in the range of 2.5 to 4 (e). Typically, we use $f = 4$, the fanout of 4 delay, or FO4 delay.

Optimizing Paths with NANDs and NORs

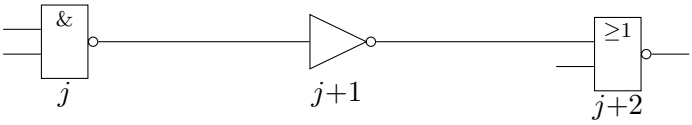


$$\text{total\_delay} = \sum_j \tau_{\text{nand}} \left(\underbrace{\frac{C_{\text{j+1}}}{C_{\text{j}}}}_{f \approx 4} + \gamma_{\text{nand}} \right)$$

$$\text{total\_delay} = \sum_j \tau_{\text{nor}} \left(\underbrace{\frac{C_{\text{j+1}}}{C_{\text{j}}}}_{f \approx 4} + \gamma_{\text{nor}} \right)$$

$$\tau_{\text{nand}} = R_{\text{eff}} C_{\text{in}} = R_{\text{eqn}} \frac{L_{\text{n}}}{W_{\text{n}}} 4 W_{\text{n}} C_{\text{g}} = 4 R_{\text{eqn}} C_{\text{g}} L_{\text{n}}$$

$$\tau_{\text{nor}} = R_{\text{eff}} C_{\text{in}} = R_{\text{eqn}} \frac{L_{\text{n}}}{W_{\text{n}}} 5 W_{\text{n}} C_{\text{g}} = 5 R_{\text{eqn}} C_{\text{g}} L_{\text{n}}$$



$$\text{total\_delay} = \tau_{\text{nand}} \left(\frac{C_{\text{j+1}}}{C_{\text{j}}} + \gamma_{\text{nand}} \right) + \tau_{\text{inv}} \left(\frac{C_{\text{j+2}}}{C_{\text{j+1}}} + \gamma_{\text{inv}} \right) + \tau_{\text{nor}} \left(\frac{C_{\text{j+3}}}{C_{\text{j+2}}} + \gamma_{\text{nor}} \right)$$

$$D_{j+1} = \tau_{\text{nand}} \left(\frac{C_{\text{j+1}}}{C_{\text{j}}} + \gamma_{\text{nand}} \right) + \tau_{\text{inv}} \left(\frac{C_{\text{j+2}}}{C_{\text{j+1}}} + \gamma_{\text{inv}} \right)$$

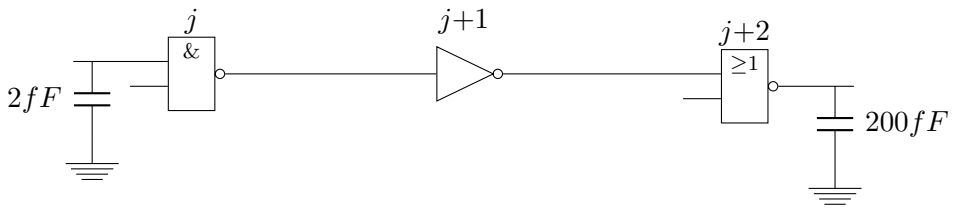
$$\frac{\delta D_{j+1}}{\delta C_{\text{j+1}}} = \tau_{\text{nand}} \frac{1}{C_{\text{j}}} - \tau_{\text{inv}} \frac{C_{\text{j+2}}}{C_{\text{j+1}}^2} = 0$$

$$\boxed{\tau_{\text{nand}} \text{FO}_{\text{j}} = \tau_{\text{inv}} \text{FO}_{\text{j+1}}}$$

$$\boxed{\tau_{\text{nand}} \text{FO}_{\text{j+1}} = \tau_{\text{inv}} \text{FO}_{\text{j+2}}}$$

To optimize the delay, we must set the fanout portion of the delay to be equal for all gates.

Computing Optimal Gate Size along a Critical Path



$$\tau_{\text{nand}} \frac{C_{\text{j+1}}}{C_{\text{in}}} = \tau_{\text{inv}} \frac{C_{\text{j+2}}}{C_{\text{j+1}}} = \tau_{\text{nor}} \frac{C_{\text{load}}}{C_{\text{j+2}}}$$

$$\begin{aligned} \text{fanout\_delay} &= \sqrt[3]{\tau_{\text{nand}} \tau_{\text{inv}} \tau_{\text{nor}} \frac{C_{\text{load}}}{C_{\text{in}}}} \\ &= \sqrt[3]{4 \cdot 3 \cdot 5 \cdot \frac{200}{2}} \cdot R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \\ &= 18.2 R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \end{aligned}$$

$$\begin{aligned} \tau_{\text{nor}} \frac{C_{\text{load}}}{C_{\text{j+2}}} &= 5 R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \frac{200fF}{C_{\text{j+2}}} = 18.2 R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \\ C_{\text{j+2}} &= 55fF \\ \tau_{\text{inv}} \frac{C_{\text{j+2}}}{C_{\text{j+1}}} &= 3 R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \frac{55fF}{C_{\text{j+1}}} = 18.2 R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \\ C_{\text{j+2}} &= 9.1fF \\ \tau_{\text{nor}} \frac{C_{\text{j+1}}}{C_{\text{in}}} &= 4 R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \frac{9.1fF}{C_{\text{in}}} = 18.2 R_{\text{eqn}} C_{\text{g}} L_{\text{n}} \\ C_{\text{j+2}} &= 2fF \end{aligned}$$

$$\begin{aligned} \text{NAND: } C_{\text{in}} = 2fF &\Rightarrow W_{\text{p}} = W_{\text{n}} = 0.5\mu m \\ \text{INV: } C_{\text{in}} = 9.1fF &\Rightarrow W_{\text{p}} = 3\mu m = 2W_{\text{n}} = 2 \cdot 1.5\mu m \\ \text{NOR: } C_{\text{in}} = 55fF &\Rightarrow W_{\text{p}} = 22\mu m = 4W_{\text{n}} = 4 \cdot 5.5\mu m \end{aligned}$$

Optimizing Paths with Logical Effort

$$\text{logical effort (LE)} = \frac{\text{intrinsic time constant of a gate}}{\tau_{\text{inv}}}$$

$$\begin{aligned}
\text{LE}_{\text{inv}} &= 1 \\
\text{LE}_{\text{nand}} &= \frac{\tau_{\text{nand}}}{\tau_{\text{inv}}} \\
\text{LE}_{\text{nor}} &= \frac{\tau_{\text{nor}}}{\tau_{\text{inv}}}
\end{aligned}$$

$$\frac{\text{total\_delay}}{\tau_{\text{inv}}} = \frac{\tau_{\text{nand}}}{\tau_{\text{inv}}}\left(\frac{C_{\text{j+1}}}{C_{\text{j}}} + \gamma_{\text{nand}}\right) + \frac{\tau_{\text{inv}}}{\tau_{\text{inv}}}\left(\frac{C_{\text{j+2}}}{C_{\text{j+1}}} + \gamma_{\text{inv}}\right) + \frac{\tau_{\text{nor}}}{\tau_{\text{inv}}}\left(\frac{C_{\text{j+3}}}{C_{\text{j+2}}} + \gamma_{\text{nor}}\right)$$

$\Leftrightarrow$

$$\begin{aligned}
D &= (\text{LE}_{\text{nand}}\text{FO}_1 + P_{\text{nand}}) + (\text{LE}_{\text{inv}}\text{FO}_2 + P_{\text{inv}}) + (\text{LE}_{\text{nor}}\text{FO}_3 + P_{\text{nor}}) \\
&= \sum(\text{LE} \cdot \text{FO} + P)
\end{aligned}$$

Wobei:

$$\begin{aligned}
\text{LE} &= \frac{\tau_{\text{gate}}}{\tau_{\text{inv}}} && \text{(logical effort)} \\
\text{FO} &= \frac{C_{\text{j+1}}}{C_{\text{j}}} && \text{(fanout, electrical effort)} \\
P &= \text{LE} \cdot \gamma_{\text{gate}} && \text{(parasitic)}
\end{aligned}$$

For the minimum delay, we need to equalize $\text{LE} \cdot \text{FO}$ for all gates!

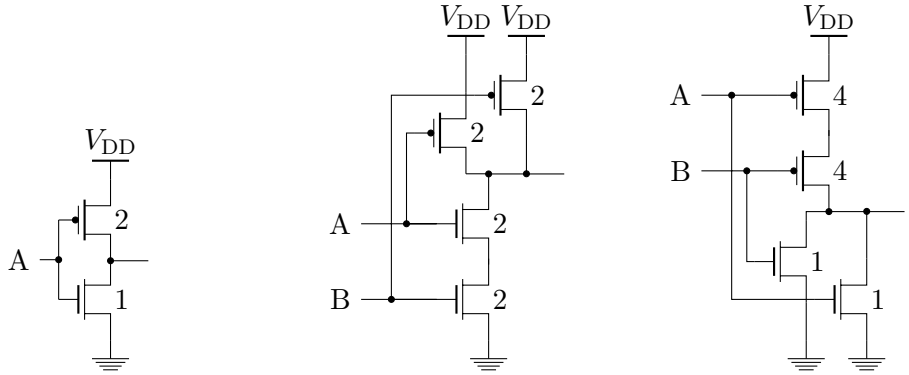
1. How do we obtain the logical effort (LE) of any type of logic gate?

$$\begin{aligned}
\tau_{\text{inv}} &= 3R_{\text{eqn}}C_{\text{g}}L_{\text{n}} \\
\tau_{\text{nand}} &= 4R_{\text{eqn}}C_{\text{g}}L_{\text{n}} \\
\tau_{\text{nor}} &= 5R_{\text{eqn}}C_{\text{g}}L_{\text{n}} \\
\text{LE}_{\text{inv}} &= 1 \\
\text{LE}_{\text{nand}} &= \frac{4}{3} \\
\text{LE}_{\text{nor}} &= \frac{5}{3}
\end{aligned}$$

   We can also use another approach to compute LE:

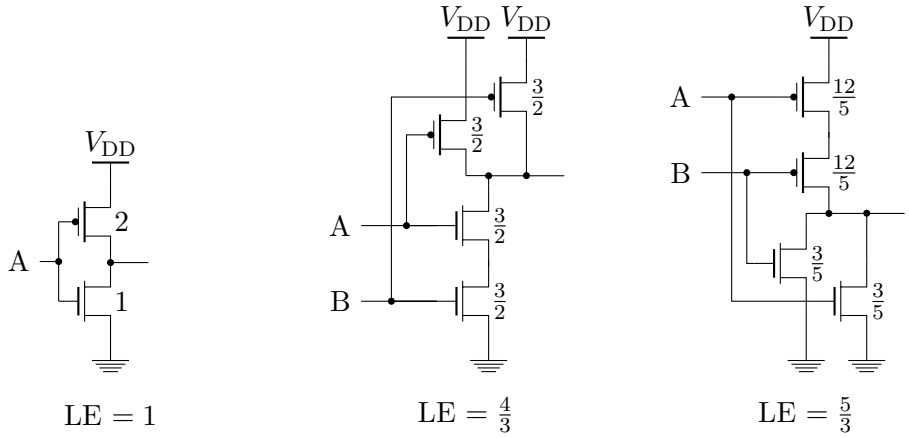
$$\begin{aligned}
\tau \cdot C_{\text{load}} &= R_{\text{eff}}C_{\text{in}}C_{\text{load}} = R_{\text{eff}}C_{\text{load}}C_{\text{in}} \\
\text{LE} &= \frac{(R_{\text{eff}}C_{\text{load}}C_{\text{in}})_{\text{gate}}}{(R_{\text{eff}}C_{\text{load}}C_{\text{in}})_{\text{inv}}}\left(= \frac{\tau_{\text{gate}}}{\tau_{\text{inv}}}\right)
\end{aligned}$$

a) Set the delays of the inverter and the gate to be the same; then take the ratio of the input capacitances, or
b) Set the input capacitances to be same; then take the delay ratio.



Logical effort for gates with equals delays (after a))

$$\left(\mathrm{LE}_{\mathrm{nand}} = \frac{(C_{\mathrm{in}})_{\mathrm{nand}}}{(C_{\mathrm{in}})_{\mathrm{inv}}} = \frac{2+2}{3} = \frac{4}{3}, \quad \mathrm{LE}_{\mathrm{nor}} \frac{4+1}{3} = \frac{5}{3}\right)$$



Logical effort using equal input capacitances (after 2))

$$R_{\mathrm{N}} \sim \frac{1}{W_{\mathrm{N}}}$$

$$\mathrm{LE}_{\mathrm{nand}} = \frac{(\frac{4}{3}R_{\mathrm{eff}})C_{\mathrm{out}}}{R_{\mathrm{eff}}C_{\mathrm{out}}} = \frac{4}{3}$$

$$\mathrm{LE}_{\mathrm{nor}} = \frac{(\frac{5}{3}R_{\mathrm{eff}})C_{\mathrm{out}}}{R_{\mathrm{eff}}C_{\mathrm{out}}} = \frac{5}{3}$$

In effect, we are taking the ratio of the driving resistance of gates that have equal input capaciatances.

A lower LE is better than a higher LE. So when we have a choice, we should use NAND gates over NOR gates.

Logical effort values of simple gates

Type	1 input	2	3	4
INV	1	-	-	-
NAND	-	$\frac{4}{3}$	$\frac{5}{3}$	$\frac{6}{3}$
NOR	-	$\frac{5}{3}$	$\frac{7}{3}$	$\frac{9}{3}$

2. How do we compute the parasitic term (P) for any type of logic gate?
   P is technology- and gate-dependent

$$P = \text{LE} \cdot \gamma = \text{LE} \cdot \frac{C'_{\text{self}}}{C'_{\text{in}}}$$

$$P_{\text{inv}} = \text{LE}\frac{C_{\text{eff}} \cdot 3W}{C_{\text{g}} \cdot 3W} = \text{LE}\frac{C_{\text{eff}}}{C_{\text{g}}} = 1 \cdot \frac{1\frac{fF}{\mu m}}{2\frac{fF}{\mu m}} = \frac{1}{2}$$

$$P_{\text{nand}} = \frac{4}{3}\frac{C_{\text{eff}}}{C_{\text{g}}} \cdot \frac{2W + 2W + 2W}{2W + 2W} = \frac{4}{3} \cdot \frac{1}{2} \cdot \frac{6}{4} = 1$$

accounting for shared S/D regions in the layout

$$P_{\text{nor}} = \frac{5}{3}\frac{C_{\text{eff}}}{C_{\text{g}}} \cdot \frac{W + 4W + 4W}{W + 4W} = \frac{5}{3} \cdot \frac{1}{2} \cdot \frac{9}{5} = 1.5$$

NAND3

$$P_{\text{nand}} = \frac{5}{3} \cdot \frac{1}{2} \cdot \frac{3 + 3 + 3 + 2 + 2}{3 + 2} = \frac{13}{6}$$

NAND4

$$P_{\text{nand}} = \frac{6}{3} \cdot \frac{1}{2} \cdot \frac{4 + 4 + 4 + 4 + 2 + 2}{4 + 2} = \frac{20}{6}$$

NOR3

$$P_{\text{nor}} = \frac{7}{3} \cdot \frac{1}{2} \cdot \frac{6 + 6 + 6 + 1 + 1}{6 + 1} = \frac{20}{6}$$

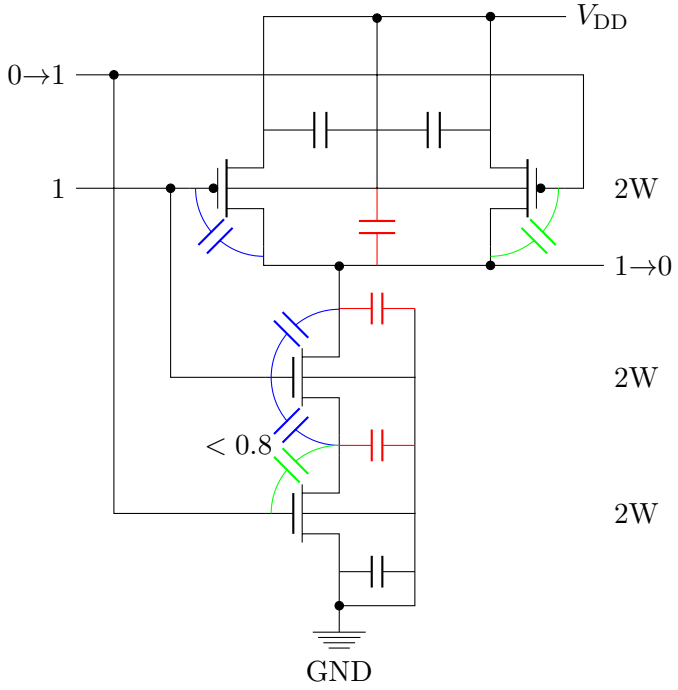
NOR4

$$P_{\text{nor}} = \frac{9}{3} \cdot \frac{1}{2} \cdot \frac{8 + 8 + 8 + 8 + 1 + 1}{8 + 1} = \frac{34}{6}$$

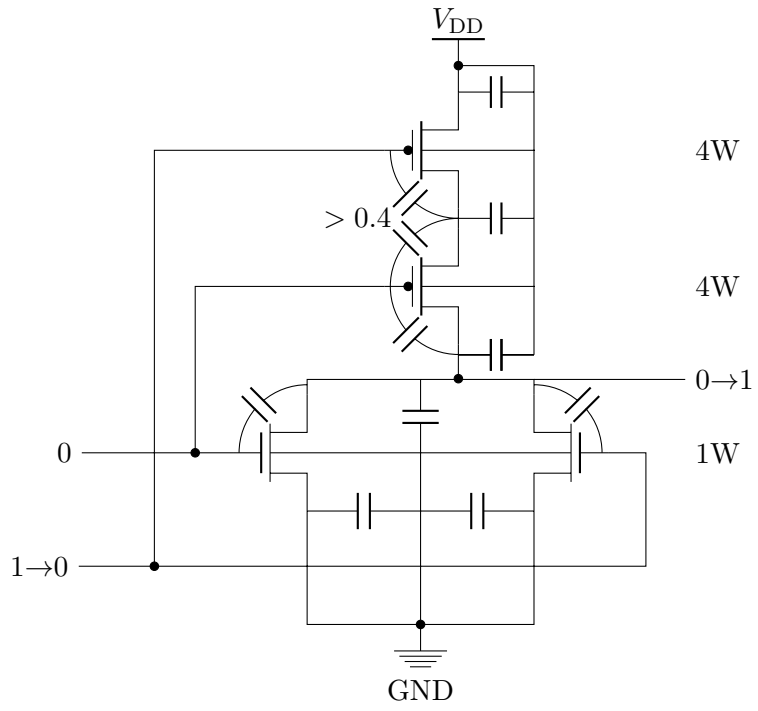
Table of parasitic terms for simple gates

Type	1 input	2	3	4
INV	0.5	-	-	-
NAND	-	1	$\frac{13}{6}$	$\frac{20}{6}$
NOR	-	1.5	$\frac{20}{6}$	$\frac{34}{6}$

(accounting for shared S/D regions in the layout), bzw genauer:



$$
\begin{aligned}
P_{\text{nand}} &= \frac{4}{3}\cdot\frac{1}{2}\cdot\frac{1}{2+2}\cdot\Big((0.5+0.5+0.25)2+ \\
&\quad +(0.5+0.25)2+(0.5+0.25)\frac{2}{3}2+0.5\cdot\frac{5}{6}\cdot 2\Big) \\
&= \frac{1}{6}\left(2.5+1.5+1+\frac{5}{6}\right) \\
&= \frac{5.8}{6}\approx 1
\end{aligned}
$$



$$
\begin{aligned}
P_{\mathrm{nor}} &= \frac{5}{3}\cdot\frac{1}{2}\cdot\frac{1}{4+1}\cdot\Bigg((0.5+0.5+0.25)1+ \\
&\quad +(0.5+0.25)4+(0.5+0.25)\frac{2}{3}4+0.5\frac{5}{6}4\Bigg) \\
&= \frac{1}{6}\left(1.25+3+2+1+\frac{2}{3}\right) \\
&= \frac{7.9}{6}\approx 1.5
\end{aligned}
$$

NAND3

$$
\begin{aligned}
P_{\mathrm{nand}} &= \frac{5}{3}\cdot\frac{1}{2}\frac{1}{2+3}\Bigg((0.5\cdot 3+0.25\cdot 2)2+(0.5+0.25)3+ \\
&\quad +(0.5+0.25\cdot 2)\cdot\frac{2}{3}\cdot 6+(0.5+0.25)\cdot\frac{2}{3}\cdot 3+0.5\cdot\frac{5}{6}\cdot 3\Bigg) \\
&= \frac{11}{6}\approx 2
\end{aligned}
$$

NAND4

$$P_{\text{nand}} = \frac{6}{3} \cdot \frac{1}{2} \frac{1}{2+4} \Big((0.5 \cdot 3 + 0.25 \cdot 3)2 + (0.5 + 0.25)4 + \\ + (0.5 + 0.25 \cdot 2) \cdot \frac{2}{3} \cdot 4 \cdot 2 + (0.5 + 0.25) \cdot \frac{2}{3} \cdot 4 + 0.5 \cdot \frac{5}{6} \cdot 4 \Big) \\ = \frac{17.5}{6} \approx 3$$

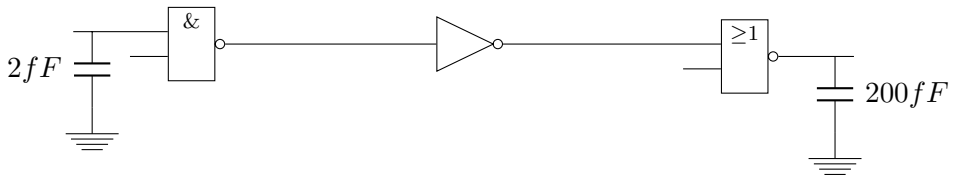
NOR3

$$P_{\text{nor}} = \frac{7}{3} \cdot \frac{1}{2} \frac{1}{6+1} \Big((0.5 \cdot 3 + 0.25 \cdot 2)1 + (0.5 + 0.25)6 + \\ + (0.5 + 0.25 \cdot 2) \cdot \frac{2}{3} \cdot 6 + (0.5 + 0.25) \cdot \frac{2}{3} \cdot 6 + 0.5 \cdot \frac{5}{6} \cdot 6 \Big) \\ = \frac{16}{6} \approx 3$$

NOR4

$$P_{\text{nor}} = \frac{9}{3} \cdot \frac{1}{2} \frac{1}{8+1} \Big((0.5 \cdot 3 + 0.25 \cdot 3)1 + (0.5 + 0.25)8 + \\ + (0.5 + 0.25 \cdot 2) \cdot \frac{2}{3} \cdot 8 \cdot 2 + (0.5 + 0.25) \cdot \frac{2}{3} \cdot 8 + 0.5 \cdot \frac{5}{6} \cdot 8 \Big) \\ = \frac{26.25}{6} \approx 4.5$$

6.6 Path Optimization Using Logical Effort



We need to equalize the LE·FO compontents of the delay for all gates:

Table of parasitic terms of simple gates

Type	1 input	2	3	4
INV	0.5	-	-	-
NAND	-	1	2	3
NOR	-	1.5	3	4.5

$$\begin{aligned}
\text{total_path_effort} &= \text{LE}_{\text{nand}} \cdot \text{LE}_{\text{inv}} \cdot \text{LE}_{\text{nor}} \frac{C_{\text{load}}}{C_{\text{in}}} \\
&= \frac{4}{3} \cdot 1 \cdot \frac{5}{3} \cdot \frac{200}{2} = 222.2 \\
\text{stage_effort} &= \sqrt[3]{222.2} = 6
\end{aligned}$$

This is the fanout portion of the delay.

$$\begin{aligned}
\text{normalized_path_delay} &= D = 3 \cdot 6 + P_{\text{nand}} + P_{\text{inv}} + P_{\text{nor}} \\
&= 18 + 1 + \frac{1}{2} + \frac{3}{2} = 21 \\
\text{min_path_delay} &= \tau_{\text{inv}} \cdot D = 7.5ps \cdot 21 = 157.5ps \\
\text{LE}_{\text{nor}} \frac{C_{\text{out}}}{C_{\text{j+2}}} &= 6 \quad \Rightarrow C_{\text{j+2}} = \frac{5}{3} \cdot \frac{200fF}{6} = 55fF \\
\text{LE}_{\text{in}} \frac{C_{\text{j+2}}}{C_{\text{j+1}}} &= 6 \quad \Rightarrow C_{\text{j+1}} = 1 \cdot \frac{55fF}{6} = 9.1fF \\
\text{LE}_{\text{nand}} \frac{C_{\text{j+1}}}{C_{\text{in}}} &= 6 \quad \Rightarrow C_{\text{in}} = \frac{4}{3} \cdot \frac{9.1fF}{6} = 2fF \quad \square
\end{aligned}$$

The minimum delay is determined without sizing the gates. If this minimum possible delay is not within specifications, the logic can be modified and the process repeated until a satisfactory solution is obtained. Once the target is achieved, gate sizing can be carried out.

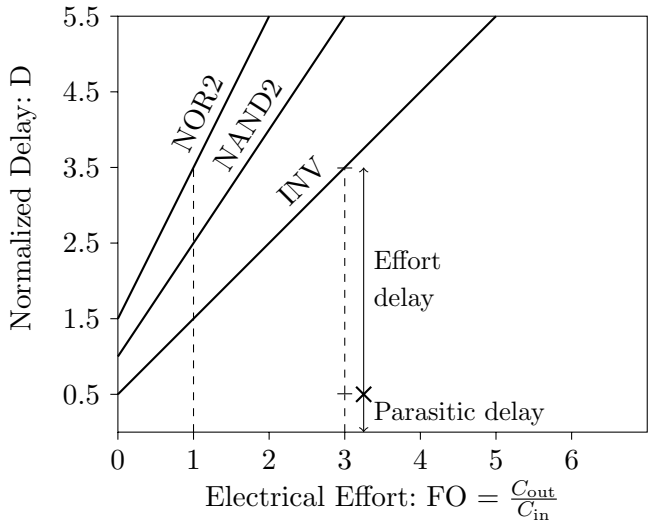
Allgemeines Prinzip

$$\begin{aligned}
\text{Problem} \rightarrow \boxed{\text{Formalisierung}} &\rightarrow \text{Modell} \\
\text{P} \rightarrow \boxed{\text{Encoder}} &\rightarrow \text{M} \\
\text{M} &\models \text{c}
\end{aligned}$$

c: Kodierung der Daten, so dass auf der 1-Menge von c operiert werden kann.
c ist eine Eigenschaft von P,
P ist eine in x kodierte Aussage $P(x)$
$[x]$ ist das Kodierungsuniversum

Ob Sie's glauben oder nicht, das ist alles Digital!

6.6.1 Understanding Logical Effort



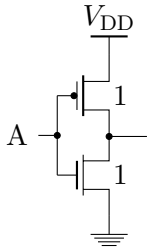
$$D = LE \cdot FO + P$$

Practical interpretation of logical effort

The electrical effort is the ratio of fanout capacitance to input capacitance.

For improved accuracy of the LE method, these plots may be obtained directly from SPICE to determine more precise values of LE and P for a given technology.

Example: LE for a Skewed Inverter



The rising and falling cases must be handled separately for this gate.

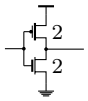
Method 1: Set the delay equal to that of the reference inverter and take the ratio of input capacitances

Falling case

$$LE_F = \frac{C_{\text{in}}|_{\text{gate}}}{C_{\text{in}}|_{\text{inv}}} = \frac{1+1}{1+2} = \frac{2}{3}$$

Rising case

$$LE_R = \frac{2+2}{1+2} = \frac{4}{3}$$



Method 2: Use the definition of logical effort (Set input capacitances equal, then take LE)

$$LE = \frac{(R_{\text{eff}} C_{\text{in}})|_{\text{gate}}}{(R_{\text{eff}} C_{\text{in}})|_{\text{inv}}}$$

Falling case

$$LE_F = \frac{(2R_{\text{eqn}})(2C_g W)}{R_{\text{eqn}}(3C_g W)} = \frac{2}{3}$$

Rising case

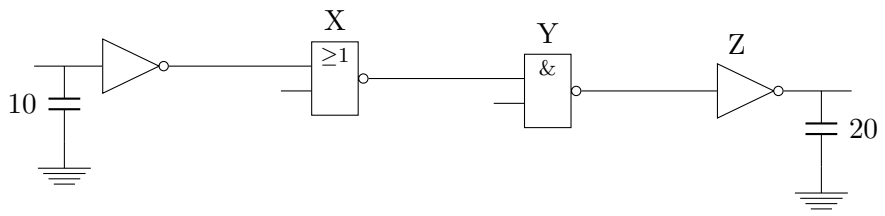
$$LE_R = \frac{(2R_{\text{eqn}})(2C_g W)}{R_{\text{eqn}}(3C_g W)} = \frac{4}{3}$$

average logical effort:

$$LE = \frac{\frac{2}{3} + \frac{4}{3}}{2} = 1$$

if required, otherwise falling and rising case separately.

Example 6.13: Path Optimization Using Logical Effort



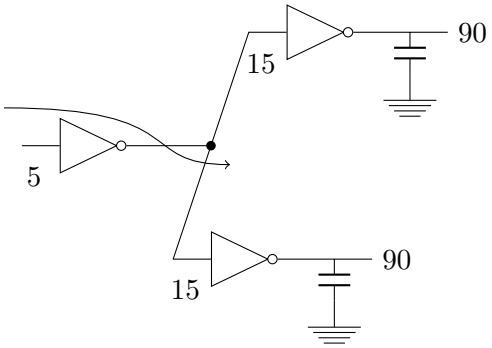
$$\begin{aligned}
\text{total_path_effort} &= \prod(\text{LE} \cdot \text{FO}) \\
&= 1\left(\frac{X}{10}\right) \cdot \frac{5}{3}\left(\frac{Y}{X}\right) \cdot \frac{4}{3}\left(\frac{Z}{Y}\right) \cdot 1\left(\frac{20}{Z}\right) \\
&= \frac{20}{9} \cdot \frac{20}{10} = \frac{400}{90} \\
\text{optimal_stage_effort: } \text{SE}^* &= \left(\frac{400}{90}\right)^{\frac{1}{4}} = 1.45 \\
\text{total_path_delay: } D &= 4\text{SE}^* + 2P_{\text{inv}} + P_{\text{nor}} + P_{\text{nand}} \\
&= 4 \cdot 1.45 + 1.0 + 1.5 + 1 = 9.3
\end{aligned}$$

The optimal value of the total path delay is known before the gate sizes have even been determined!

$$\begin{aligned}
\text{SE}^* &= \text{LE} \times \text{FO} = \text{LE} \cdot \frac{C_{\text{out}}}{C_{\text{in}}} \\
C_{\text{in}} &= \text{LE}\left(\frac{C_{\text{out}}}{\text{SE}^*}\right) \qquad \text{working backwards} \\
Z &= 1 \cdot \left(\frac{20}{1.45}\right) = 13.8 \\
Y &= \frac{4}{3} \cdot \left(\frac{Z}{1.45}\right) = 12.7 \\
X &= \frac{5}{3} \cdot \left(\frac{Y}{1.45}\right) = 14.5 \\
C_{\text{in}} &= 1 \cdot \left(\frac{14.5}{1.45}\right) = 10 \quad \square
\end{aligned}$$

The first inverter size can be verified by the last equation, which is consistent with the specified input capacitance value.

Branching Effort and Sideloads

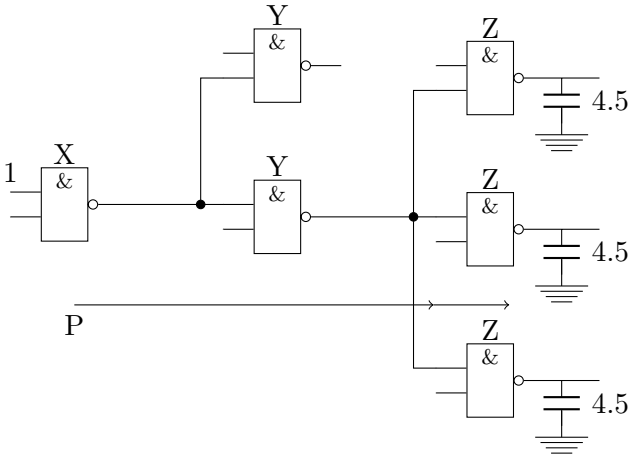


Branching Factor:
Sideload

The branch is identical to the path of interest

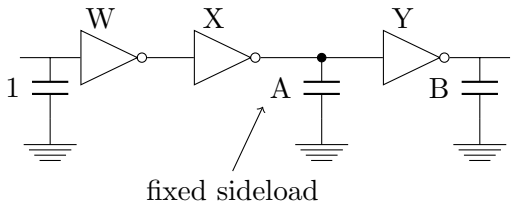
$$\text{total\_path\_effort} = \prod (\text{LE} \cdot \text{BE} \cdot \text{FO}) = \prod (\text{LE} \cdot \text{BE}) \cdot \frac{C_{\text{load}}}{C_{\text{in}}}$$

Example 6.15



$$\text{logical\_effort: } \mathrm{LE_p} = \left(\frac{4}{3}\right)^3$$
$$\text{electrical\_effort: } \mathrm{FO_p} = \frac{C_{\text{out}}}{C_{\text{in}}} = 4.5$$
$$\text{branching\_effort: } \mathrm{BE_p} = 2 \cdot 3 = 6$$
$$\text{path\_effort: } \mathrm{PE} = \mathrm{LE_p} \cdot \mathrm{BE_p} \cdot \mathrm{FO_p} = 64$$
$$\text{optimal\_stage\_effort: } \mathrm{SE}^* = (\mathrm{PE})^{1/3} = 4$$
$$\text{Delay (normalized): } D = N \cdot \mathrm{SE}^* + \text{Parasitics} = 3 \cdot 4 + 3 \cdot 1 = 15$$
$$C_{\text{in}} = \mathrm{BE} \cdot C_{\text{out}} \frac{\mathrm{LE}}{\mathrm{SE}^*}$$
$$z = 1 \cdot 4.5 \frac{4/3}{4} = 1.5$$
$$y = 3 \cdot 1.5 \frac{4/3}{4} = 1.5$$
$$x = 2 \cdot 1.5 \frac{4/3}{4} = 1$$

Computing Delay with Sideloads Example 6.16



Without sideload and FO4 sizing rules:
$w = 1, x = 4, y = 16 \Rightarrow$ Minimum delay
First two stages:

$$D_1 = \mathrm{LE_{inv}}\left(\frac{x}{w} + \gamma_{\text{inv}}\right) + \mathrm{LE_{inv}}\left(\frac{A+y}{x} + \gamma_{\text{inv}}\right)$$
$$\frac{\delta D_1}{\delta x} = \frac{1}{w} - \frac{A+y}{x^2} = 0 \Leftrightarrow \frac{x}{w} = \frac{A+y}{x}$$

Next two stages:

$$D_2 = \mathrm{LE_{inv}}\left(\frac{A+y}{x} + \gamma_{\text{inv}}\right) + \mathrm{LE_{inv}}\left(\frac{B}{y} + \gamma_{\text{inv}}\right)$$
$$\frac{\delta D_2}{\delta y} = \frac{1}{x} - \frac{B}{y^2} = 0 \Leftrightarrow \frac{y}{x} = \frac{B}{y}$$

We can use the two equations to iterate the solution:

$$y^2 = BX, y = \sqrt{BX} = \sqrt{64 \cdot 4} = 16$$

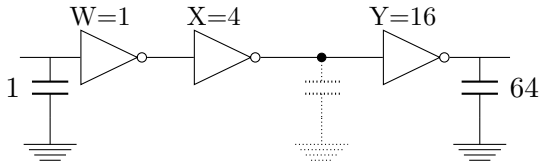
$$x^2 = (A + y)w, x = \sqrt{(A + y)w} = 4.9$$

$$(y = 17.7) \Rightarrow (x = 5.1)$$

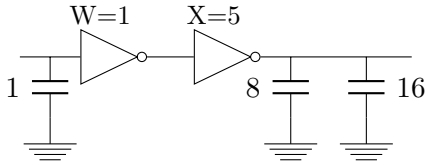
$$(y = 18) \Rightarrow (x = 5)$$

Alternative approach less prone to error:

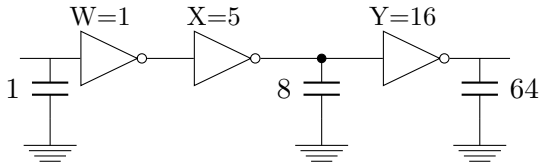
a) Using logical effort without the sideload
b) Add in the sideload and the loading of the next gate
c) Remove downstream gates and solve with LE
d) Combination (of above)



a)



b) + c)



d) combination

Slightly different but muh easier to carry out, hand calcuation using this method compared to the iterative approach.

Logical effort is a useful tool for back of the envelope timing optimization:

- Allows quickly to determine the optimal delay for a given path, and
- the corresponding device sizes to achieve this delay

- it provides insight into the key factors in the delay of logic paths

There are many other aspects of logical effort that were not covered in this chapter (See Sutherland, 1999).

7 Transfer Gate and Dynamic Logic Design

Static Logic Gates

- CMOS
  - dissipates far less power
  - more area due to complementary PMOS and their size requirements to achieve equal rise / fall delays (2:1)
- Pseudo-NMOS
  - require ratioed devices to set the desired value of V_{oL} (1:4)
  - asymmetric rise and fall times

Key paramters are area, timing and power. All nodes of a static gate have direct paths to V_{DD} or Gnd. So long as the power remains on, the value of the output node is held indefinitely.

Dynamic Gates

- Store their value on a capacitor
- Storage nodes isolated for a long period of time
  - $\Rightarrow$ May decay, if not refreshed or updated periodically
  - $\Rightarrow$ More susceptible to noise events
- Can outperform static logic gates
- Transfer gates (1,0,Z), in high-impedance state, the previous value is stored as charge on the output capacitance
- Additional clocking signals for porper operations precharged to an initial value on one part of the clock cycle, evaluating their correct output values on the other part of of the cycle

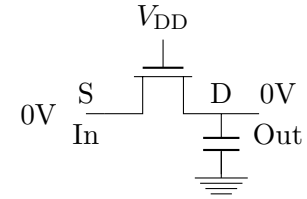
Basic Concepts

- Pass transistor
- Charge sharing
- Feedthrough
- Charge leakage

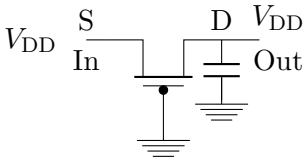
Pass Transistor

- on: transfer the input signal
- off: output enters the high-Z state (to hold its previous value)

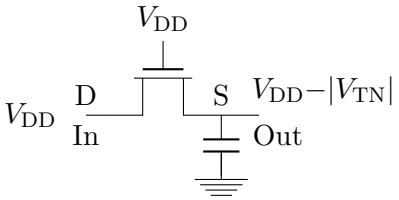
- 3 terminals: input, output, control
- NMOS has trouble to pass V_{DD}
- PMOS has trouble to pass $0V$



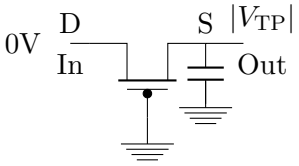
a) entladen



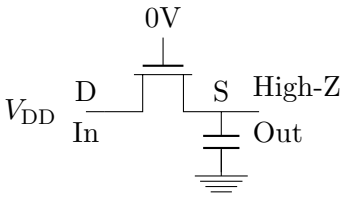
b) laden



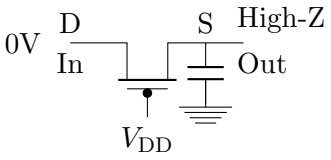
c) laden



d) entladen

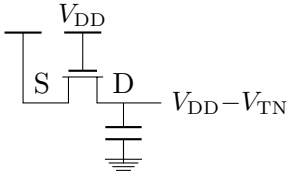


e)

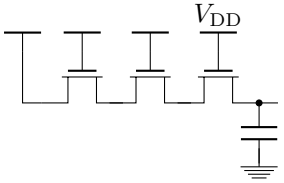


f)

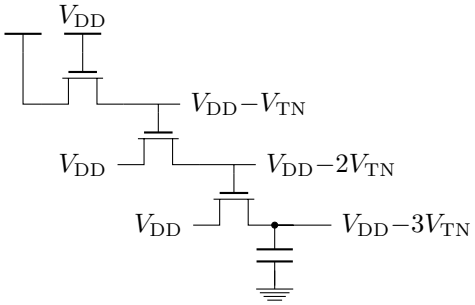
- for NMOS, the drain is the higher of the two nodes
- for PMOS, the source is the higher of the two nodes



a)

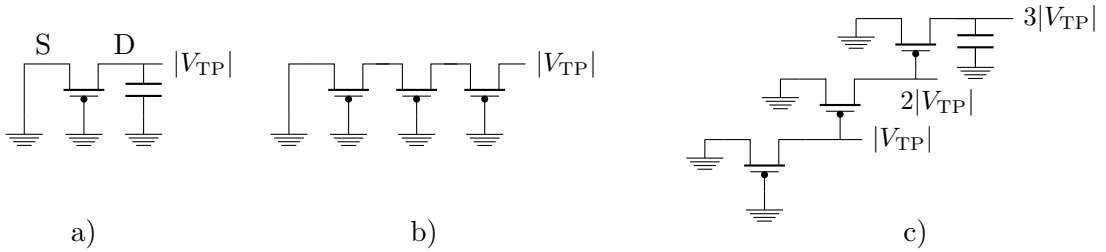


b)



c) Kaskode

NMOS pass gate configurations (ignoring body effect)

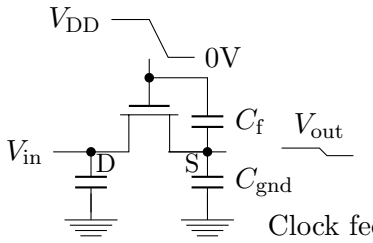


a) b) c)

PMOS pass gate configurations (ignoring body effect)
The designers should avoid using the output of a pass transistor to drive the gate of another pass transistor.

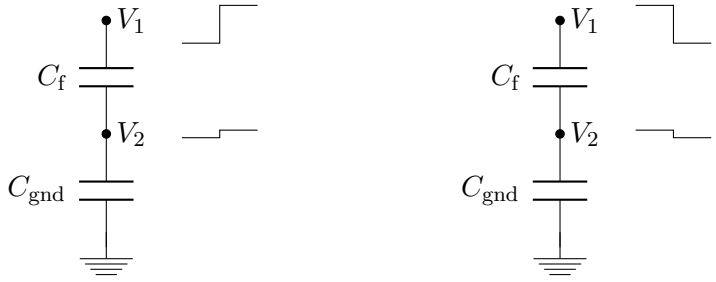
7.1 Capacitive Feedthrough

C_f causes the clock signal to feed through to the output.



Clock feedtrough

The charges associated with the two capacitors C_f and C_{gnd} redistribute to maintain equality (displacement current).
The same effect would be observed at the drain node if it were isolated from the rest of the circuit.



a) positive feedthrough b) negative feedthrough

The charge at the external node 1 produces a replica change at the internal node 2

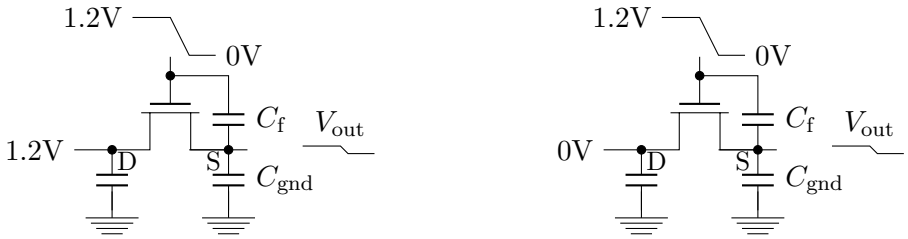
which is a high-Z node.

$$C_{\mathrm{f}}(V_1 - V_2) = C_{\mathrm{gnd}}V_2$$
$$V_2 = \frac{C_{\mathrm{f}}V_1}{C_{\mathrm{f}} + C_{\mathrm{gnd}}}$$
$$\Delta V_2 = \frac{C_{\mathrm{f}}}{C_{\mathrm{f}} + C_{\mathrm{gnd}}}\Delta V_1 \tag{7.3}$$

Bootstrapping is usually associtated with increasing a node voltage above V_{DD} using active devices. We use the term here more generally to refer to any increase in the voltage due to series capacitor effects.

$$C_{\mathrm{f}} = C_{\mathrm{gs}}, C_{\mathrm{gnd}} = C_{\mathrm{BS}} + C_{\mathrm{load}}, C_{\mathrm{gnd}} \gg C_{\mathrm{f}}$$

V_{T} Drop and Clock Feedthrough Effects ($4\lambda/2\lambda$)



Initial:

$$V_{\mathrm{out}} = V_{\mathrm{DD}} - V_{\mathrm{TN}}(V_{\mathrm{out}}) = 1.2 - (0.4 + 0.2(\sqrt{0.88 + V_{\mathrm{out}}} - \sqrt{0.88}) = 0.73V$$

Switch from high to low:

$$V_{\mathrm{out}} = 0.73 - \Delta V = 0.73 - \frac{C_{\mathrm{f}}}{C_{\mathrm{f}} + C_{\mathrm{gnd}}} \cdot 1.2$$
$$C_{\mathrm{f}} = C_{\mathrm{OL}} = C_{\mathrm{OL}} = C_{\mathrm{ol}}W = (0.25\frac{fF}{\mu m}) \cdot 0.2\mu m = 0.05fF$$
$$C_{\mathrm{gnd}} = C_{\mathrm{eff}} \cdot W = (1\frac{fF}{\mu m}) \cdot 0.2\mu m = 0.2fF$$
$$V_{\mathrm{out}} = 0.73 - \frac{0.05 \cdot 1.2}{0.05 + 0.2} \approx 0.5V$$

(Badly, below typical switching threshold, if no additional C_{out})

$$V_{\mathrm{out}} = 0V(\text{linear region})$$
$$C_{\mathrm{f}} = \frac{1}{2}C_{\mathrm{g}}W + C_{\mathrm{ol}}W = 0.5(2fF/\mu m)0.2\mu m + (0.25fF/\mu m) \cdot 0.2\mu m = 0.25fF$$
$$V_{\mathrm{out}} = 0 - \frac{C_{\mathrm{f}}(1.2)}{C_{\mathrm{f}} + C_{\mathrm{gnd}}} = 0 - \frac{0.25(1.2)}{0.25 + 0.2} = -0.67V$$

The devices does not shut off until $V_{\mathrm{GS}} \leq V_{\mathrm{TN}}$.
The feedthrough equation is intended for use at high-Z nodes only.

7.2 Charge Sharing

Two isolated nodes with different voltage levels are suddenly connected together when a pass transistor turns on.

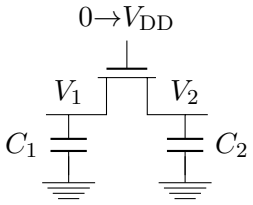
a) Before b) After

$$Q_{\text{total}} = C_1V_1 + C_2V_2 = (C_1 + C_2V^*)$$
$$V^* = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} \tag{7.6}$$

To reduce charge sharing ($V^* < V_2$), C_2 should be made much larger than C_1.

$$\text{Achtung! } V^* > V_{\text{DD}} - V_{\text{TN}} \Rightarrow \begin{cases} V_1 = V_{\text{DD}} - V_{\text{TN}} \\ Q_2 = Q_{\text{total}} - C_1(V_{\text{DD}} - V_{\text{TN}}) \\ V_1 \neq V_2 \text{ after charge sharing} \end{cases}$$

Example:



a) $C_1 = 100fF$
$C_2 = 20fF$
$V_1 = 0V$
$V_2 = 1.2V$
$\Rightarrow V^* = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} = 0.2V$

b) $C_1 = 20fF$
$C_2 = 20fF$
$V_1 = 0V$
$V_2 = 1.2V$
$\Rightarrow V^* = 0.6V$

c) $C_1 = 20fF$
$C_2 = 100fF$
$V_1 = 0V$
$V_2 = 1.2V$
$\Rightarrow V^* = 1.0V$

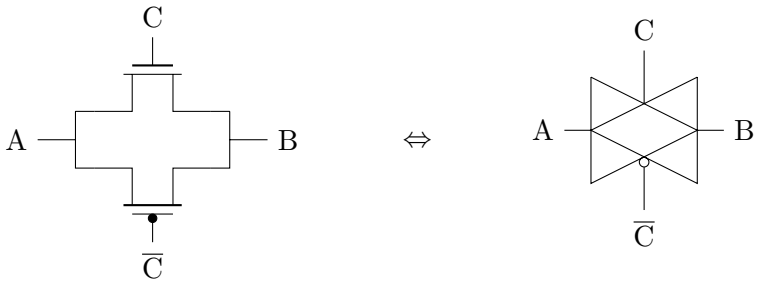
V_1 cannot rise above $0.8V$

$Q_1 = 0.8V \cdot 20fF = 16fC$
$Q_2 = (120 - 16)fC = 104fC$
$V_2 = \frac{104fF}{100fF} = 1.04V$

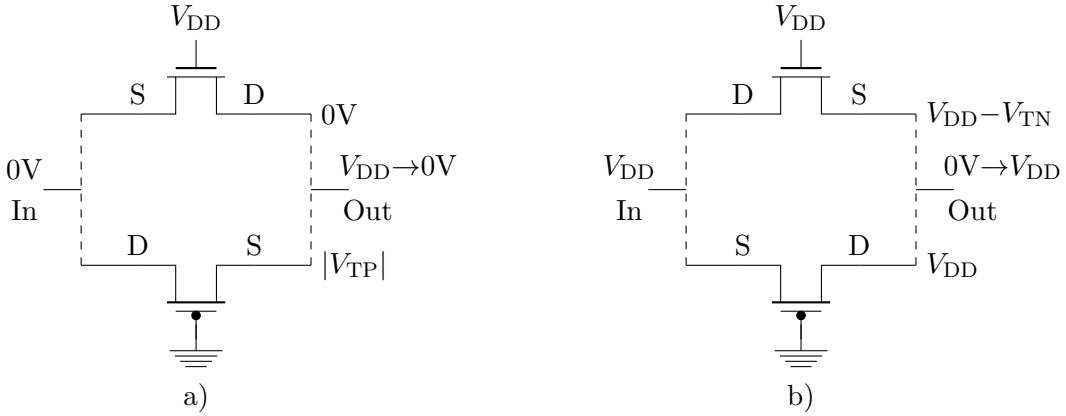
Other sources of charge loss

- reverse-bias leakage current from the drain junction and subthreshold current
- noise injection from neighboring wires
- α-particles as a leading cause of so-called **soft errors**

CMOS Transmission Gate Logic



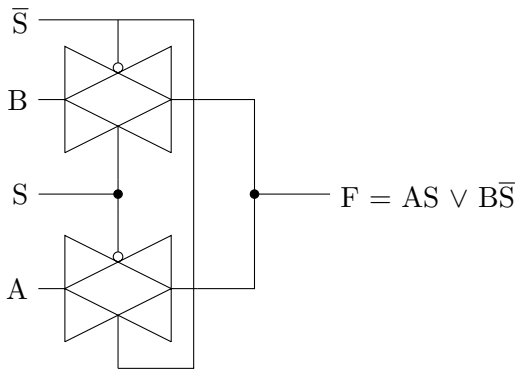
The cost of this feature is not only an extra transistor, but also an extra inverter since each transistor requires a complementary control input (4 transistors).



Transmitting low and high signals (0V, V_{DD})
The degree of capacitive feedthrough is reduced.

Multiplexers Using CMOS Transfer Gates

CMOS transmission gate logic can be used to reduce the number of transistors needed to implement certain logic functions.

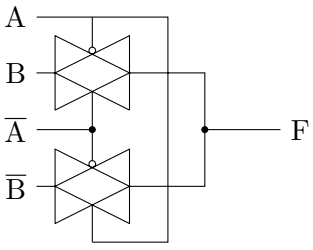


S	A	B	F
0	Z	B	B
1	A	Z	A

Multiplexer Configuration - Analog Transmit

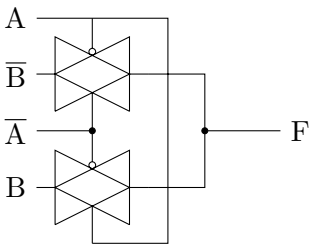
mit S=A
$\Rightarrow$ F = $\overline{A}$B ∨ A$\overline{B}$

S	F
0	B
1	$\overline{B}$

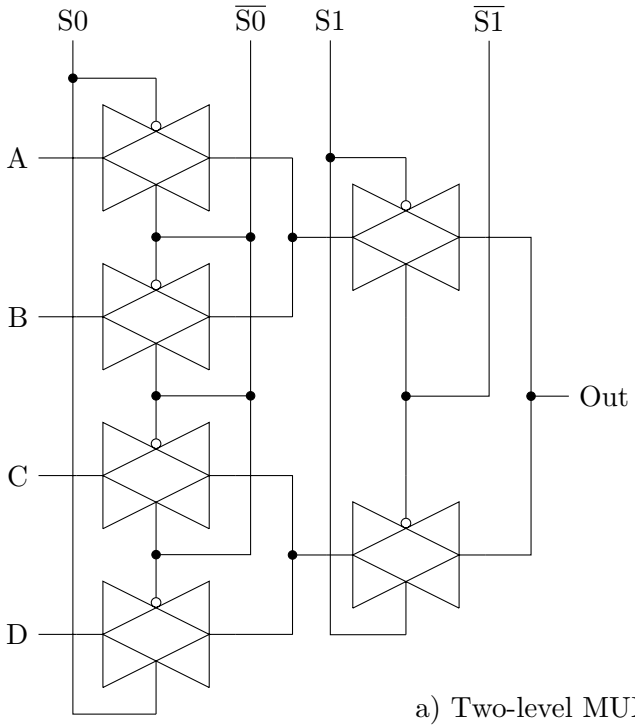


a) XOR Gate (8 transistors)
- contrary to 16 transistors in CMOS

mit S= $\overline{A}$
$\Rightarrow F = AB \vee \overline{AB}$

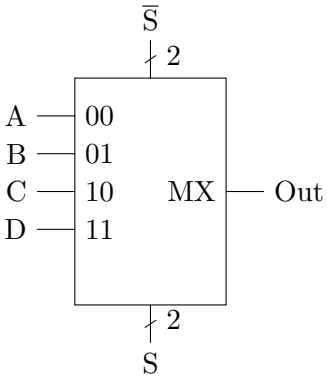


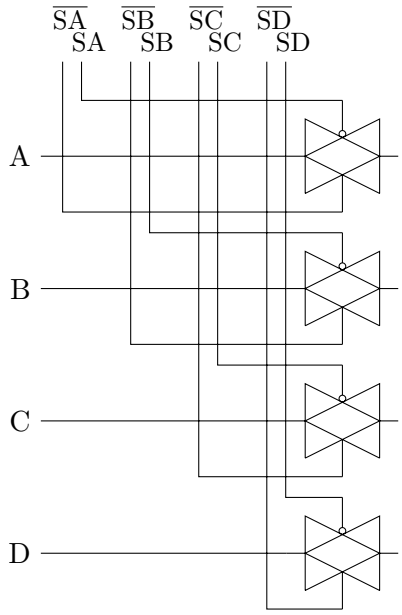
b) XOR Gate

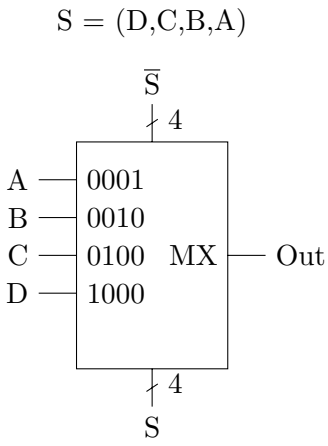


a) Two-level MUX

$S = (S_1S_0)$



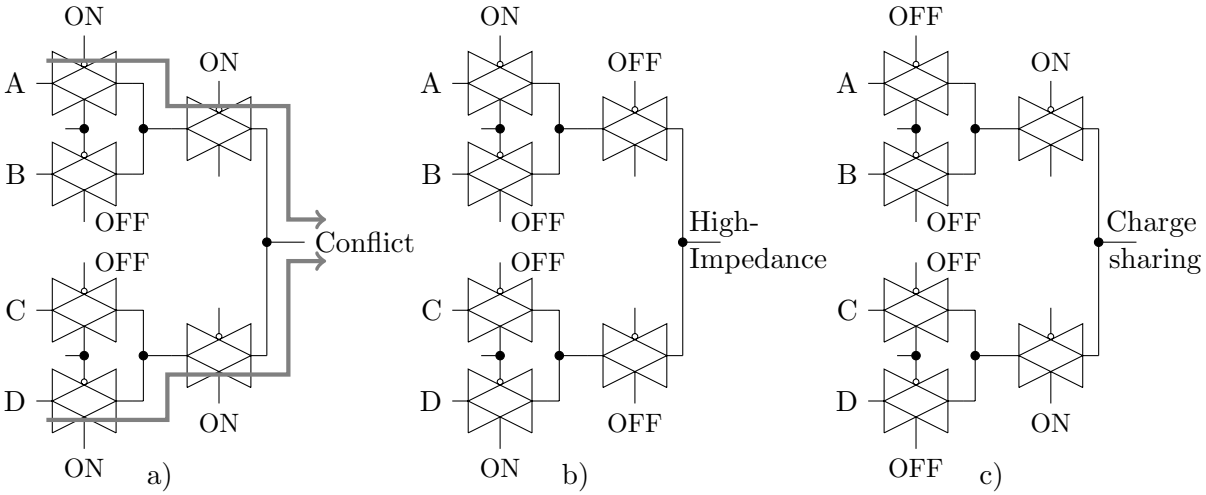




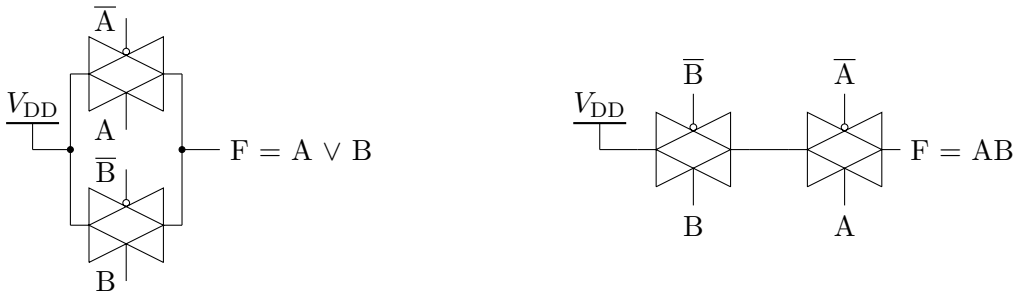
b) single-level MUX

one-of-four MUX

Improper conditions for multiplexer style logic



- the data inputs to the multiplexer must all be valid
- the control signals must turn on only one path at a time



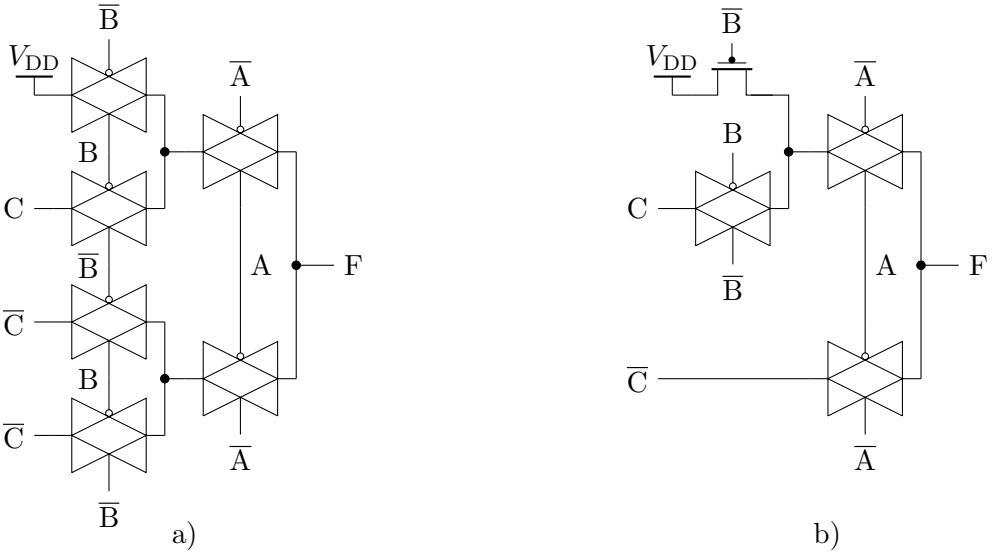
a) b)

OR and AND functions using CMOS transmission gates (AA)
$F = AB \vee A\overline{B}C \vee \overline{AC}$

- Identify A and B as control signals and build a truth table

A	**B**	**F**
0	0	$\overline{C}$
0	1	$\overline{C}$
1	0	C
1	1	1

- Convert the truth table to a multiplexer-style design by creating a signal path in the circuit for each row of the truth table. Any AA of Fig. 7.13 can be used.
- Combine paths or remove unnecessary transistors



a) b)

$F = \overline{A}B \vee A\overline{B}$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

SA Kombinatorik

=

A	F
0	*
0	*
1	$\overline{B}$
1	$\overline{B}$

AA MUX

+

A	F
0	B
0	B
1	*
1	*

AA MUX

=

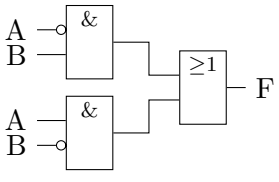
B	F
0	A
1	*
0	A
1	*

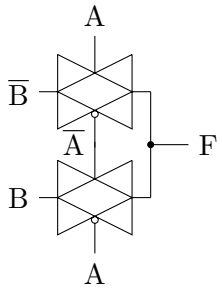
AA MUX

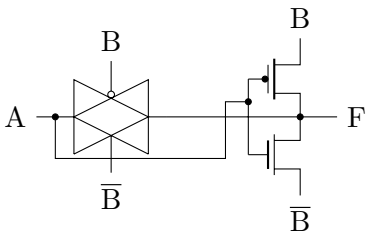
+

A	F
0	*
0	B
1	*
1	$\overline{B}$

AA INV

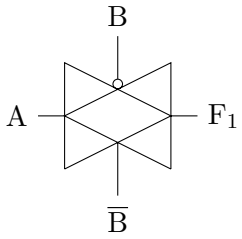






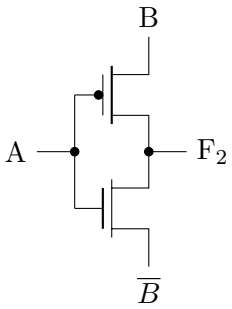
$F = A\overline{B} + \overline{A}B$

$F_1 = A\overline{B}$



A	**B**	**F1**
0	0	A
0	1	Z
1	0	A
1	1	Z

$F_2 = \overline{A}B + \overline{A}\overline{B}$

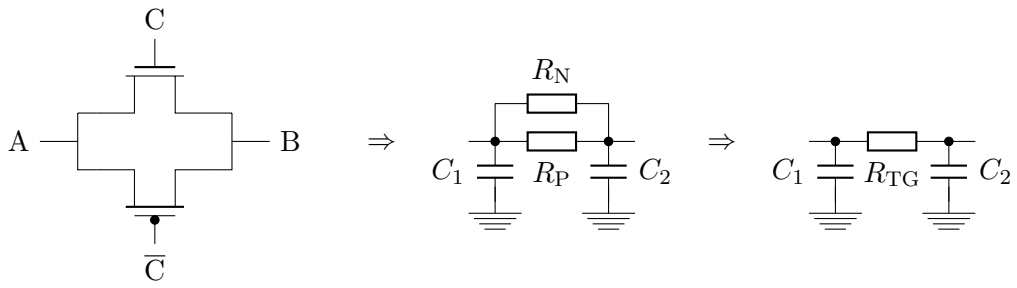


A	**B**	**F2**
0	0	Z
0	1	B
1	0	Z
1	1	$\overline{B}$

$F = F_1 + F_2$

A	**B**	F_1	F_2	**F**	**F**
0	0	A	Z	A	0
0	1	Z	B	B	1
1	0	A	Z	A	1
1	1	Z	$\overline{B}$	$\overline{B}$	0

7.2.1 CMOS Transmission Gate Delay

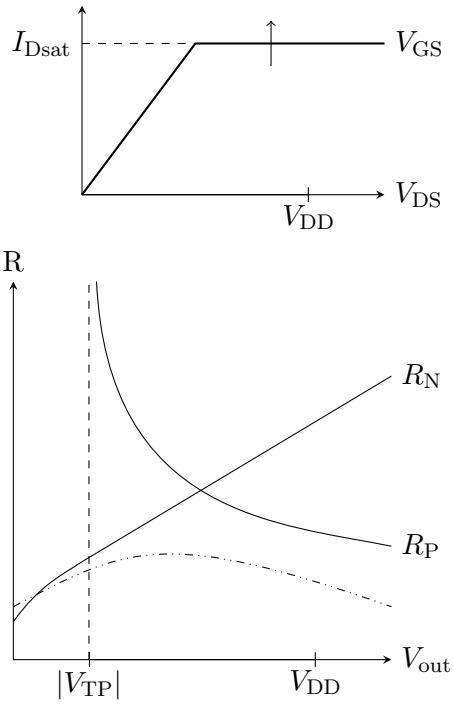


RC model for CMOS transmission gate

The role of the TG is to transmit signals from input to output under gate control.

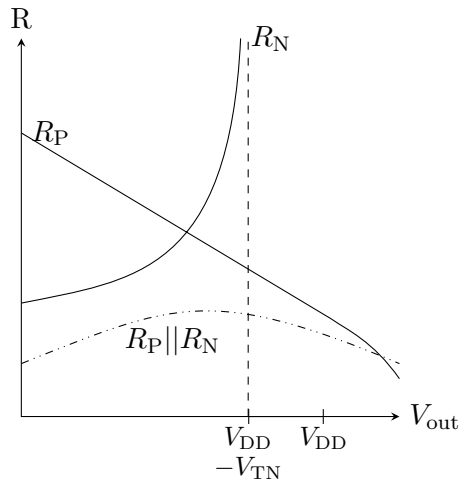
$$\boxed{R_{on} \approx \frac{V_{DS}}{I_{ds}}}$$

output: $V_{DD} \rightarrow 0V$



$$R_N = \frac{V_{out}}{I_{Dsat,n}}$$
$$R_N = \frac{V_{out}}{I_{Dlin,n}}$$
$$R_P = \frac{V_{out}}{I_{Dsat,p}}$$

output: $0V \rightarrow V_{DD}$



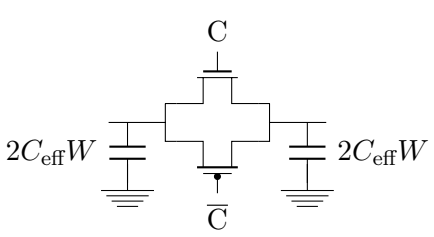
$$R_P = \frac{V_{DD} - V_{out}}{I_{Dsat,p}}$$
$$R_P = \frac{V_{DD} - V_{out}}{I_{Dlin,p}}$$
$$R_N = \frac{V_{DD} - V_{out}}{I_{Dsat,n}}$$

It is convenient to model this resistance by a constant value based on the average during the transition.

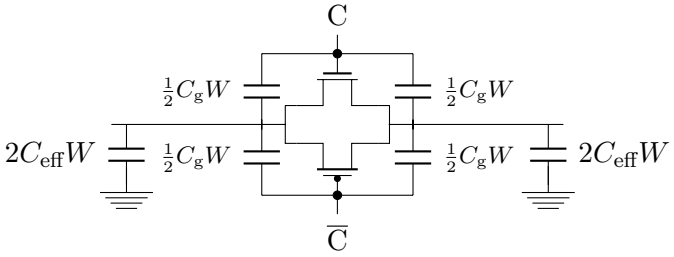
$$R_{TG}(0 \to V_{DD}) = R_N||R_P \approx 2R_{eqn}||R_{eqp}$$
$$2R_{eqn}||2.4R_{eqp} = 1.1R_{eqn} \approx R_{eqn}$$

$$R_{TG}(V_{DD} \to 0) = R_N||R_P \approx R_{eqn}||2R_{eqp}$$
$$R_{eqn}||4.8R_{eqp} = 0.83R_{eqn} \approx R_{eqn}$$

$$\Rightarrow R_{TG} = R_{eqn}\frac{L}{W}$$



OFF state



ON state

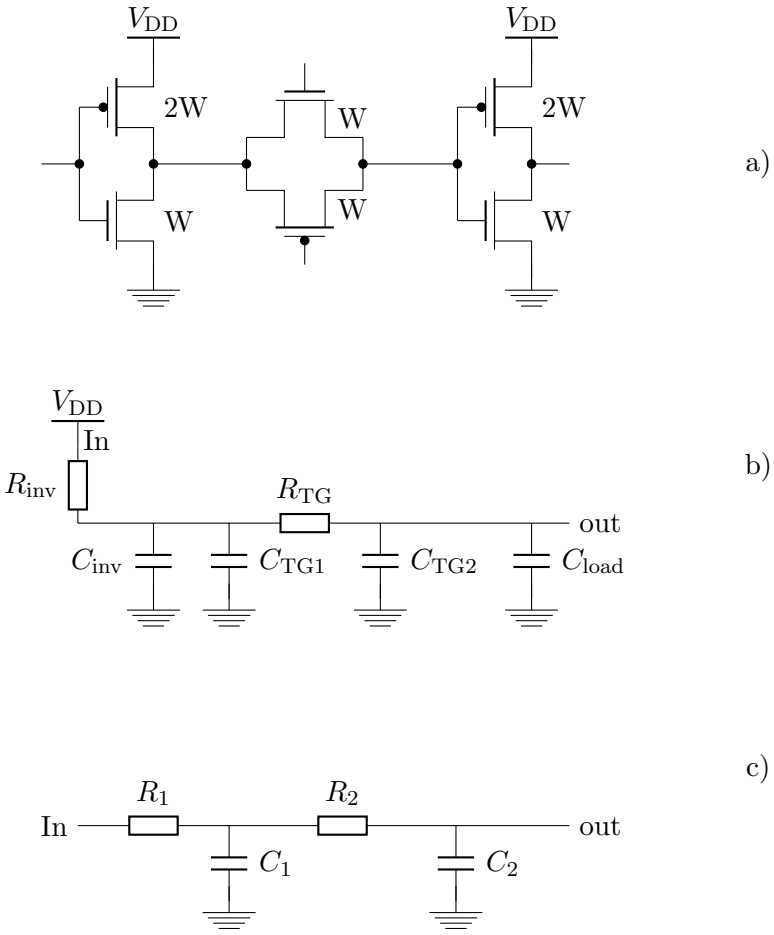
Except for the overlap capacitances, from a) follows

$$C_{in} = C_{out} = C_{eff}(W_n + W_p) = C_{eff}2W$$

In the on state the devies are assumed to be in the linear region (which is true for some part of the transition for both devies)

$$C_{in} = C_{out}C_{eff}(W_n + W_p) + \frac{1}{2}(C_gW_n + C_gW_p) = C_{eff}2W + C_gW$$

With the complete RC model defined as above, it is now possible to compute the path delay of circuits containing transmission gates.
However, accurate delay calculation must involve the characteristics of the driver and load of the transmission gate.

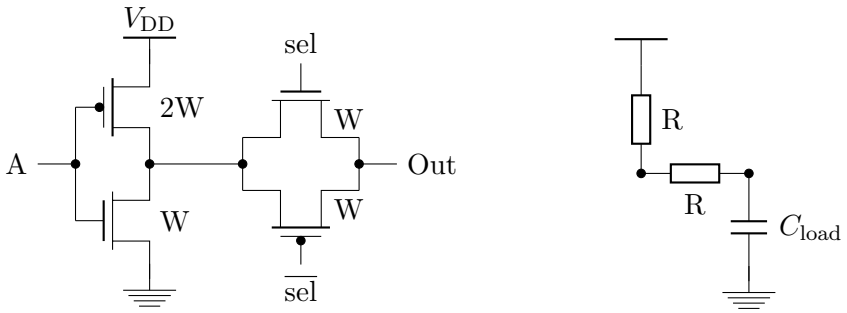


Transmission gate with driver and load

Elmore Delay (Chapter 10)

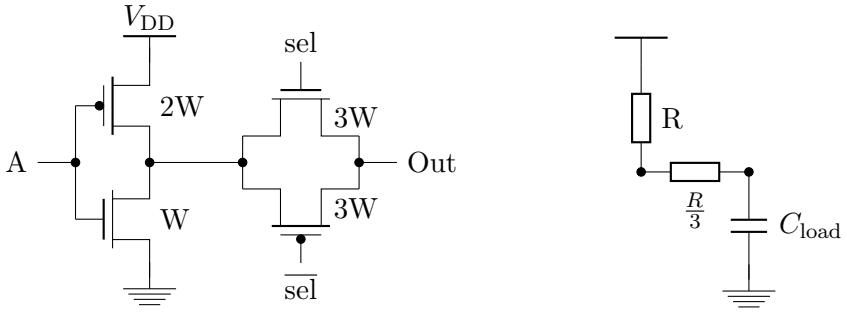
$$\begin{aligned} t_{\text{Elmore}} &= R_1C_1 + (R_1 + R_2)C_2 \\ &= R_{\text{inv}}(C_{\text{inv}} + C_{\text{TG1}}) + (R_{\text{inv}} + R_{\text{TG}})(C_{\text{TG2}} + C_{\text{load}}) \end{aligned}$$

7.2.2 Logical Effort with CMOS Transmission Gates



This is another type of tristate driver which performs a similar function to the trisate inverter seen in Section 4.9 of Chapter 4. Here, we have three inputs: `A`, `sel`, $\overline{\texttt{sel}}$

$$\text{LE input A} = \frac{3WC_g(2R)}{3WC_gR} = 2$$
$$\text{LE input sel} = \frac{WC_g(2R)}{3WC_gR} = \frac{2}{3}$$



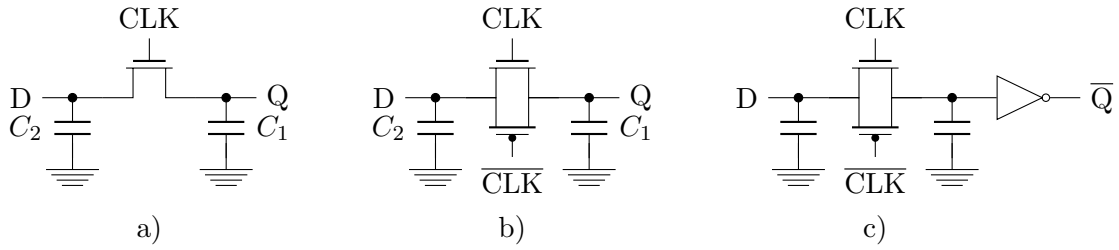
LE computation with a 3X transmission gate

$$\text{LE input A} = \frac{3W(4R/3)}{3WR} = \frac{4}{3}$$
$$\text{LE input sel} = \frac{3W(4R/3)}{3WR} = \frac{4}{3}$$

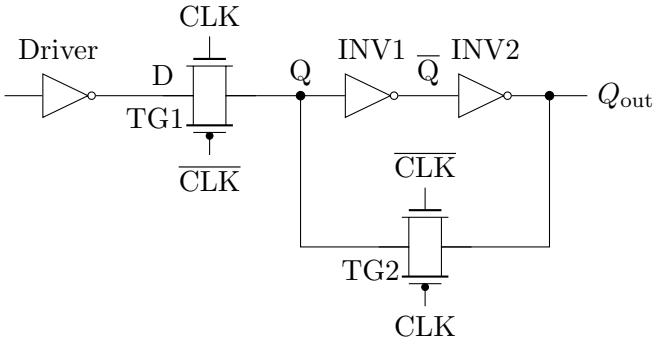
`input A` experiences a smaller output resistance without any change in its input capacitance, while `input sel` experiences an increase of three times its input capacitance but not a reduction of three times its output resistance.

7.3 Dynamic D-Latches and D-FlipFlops

Requires fewer transistors



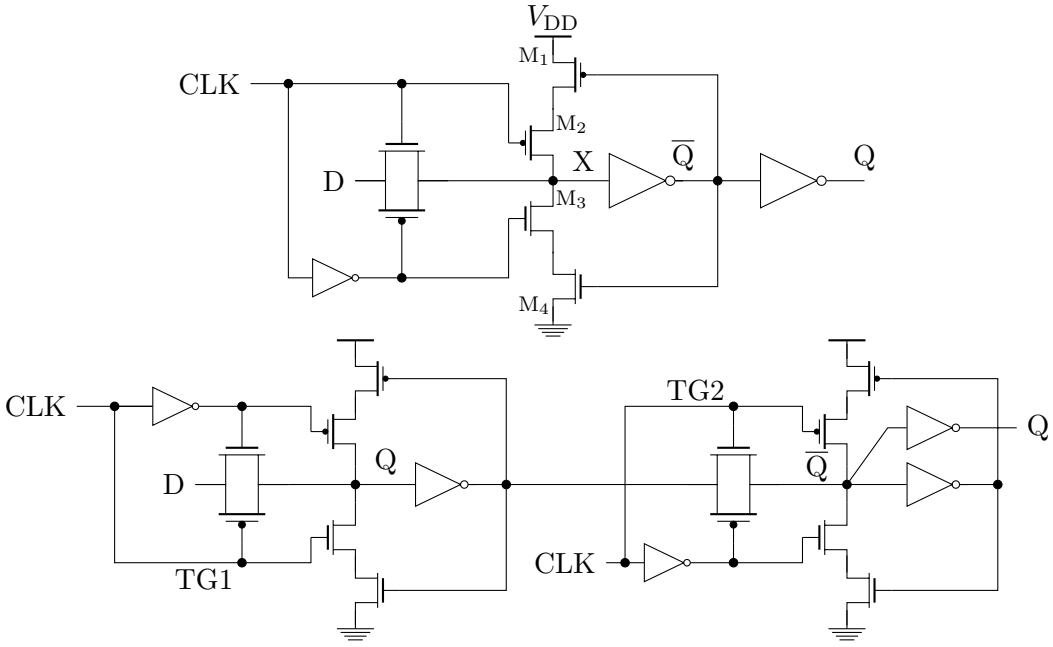
- the voltage at the output can only rise to $V_{\text{DD}} - V_{\text{T}}$
- clock feedthrough at Q when the clock goes low
- no $\overline{Q}$ output available
- the high-Z state after the clock goes low is susceptible to all of the charge loss mechanisms



- TG1 is on when we are in transparent mode
- TG2 is on when we are in hdd mode

When the circuit is in transparent mode, TG2 is off and the value of D passes through to Q_{out} after a delay of TG1 and two inverters.

While this circuit removes the problem of dynamic storage it introduces another small problem. When the CLK signal goes high, we note that there is a delay before $\overline{\text{CLK}}$ goes low. In that situation, the n-channel device of TG2 is still on. If D is different from the previously stored Q, then there will be a conflict at node Q for a short duration. TG1 is attempting to apply a new a value at Q while TG2 is reciculating the old value through the loop. The problem can be resolved with proper sizing of the INV2, TG2, TG1 and the gate that is driving D. The basic idea is to ensure that the forward path is stronger than the feedback path.



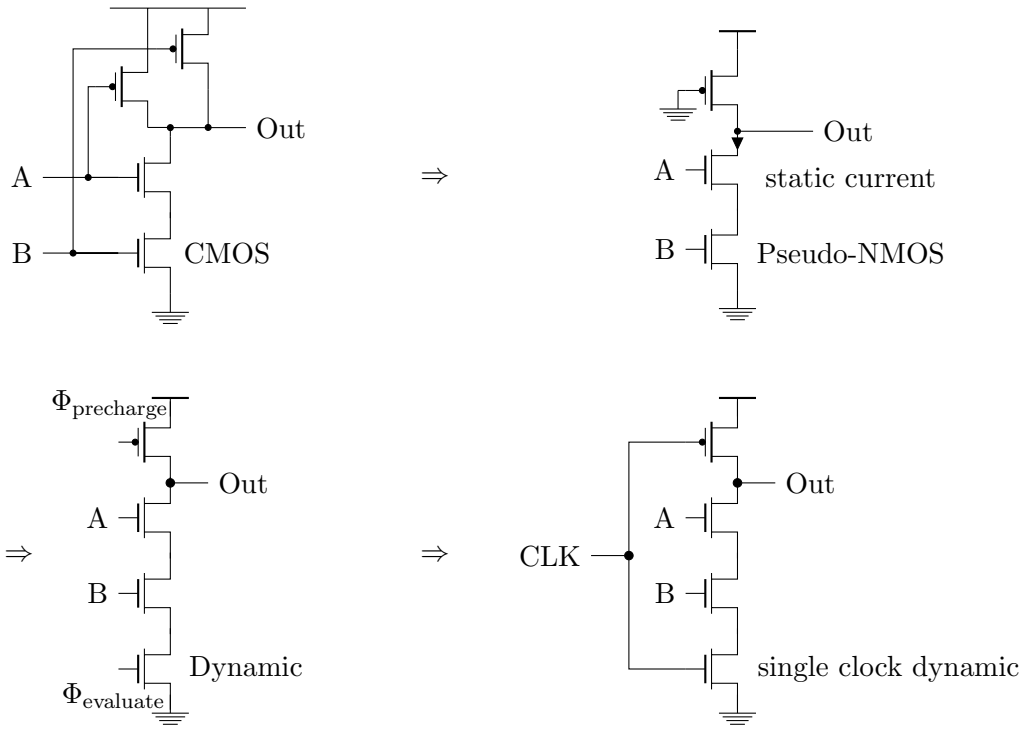
7.4 Domino Logic

Numerous difficulties with dynamic logic:

- charge sharing
- feedthrough
- charge leakage
- single-event upsets (kurzer Glitch durch α-Teilchen Einstrahlung $\Rightarrow$ kann dynamisches Bauteil kurzzeitig logisch verndern; findet man nie wieder)

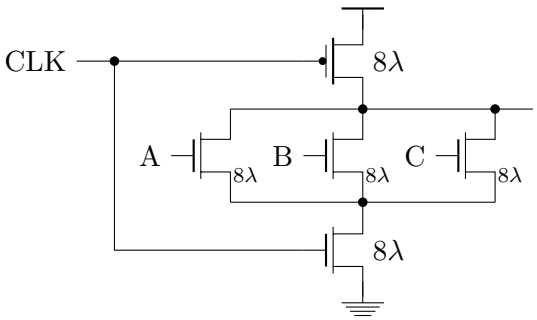
vs static logic:

- PMOS devices with relatively large sizes
- Pseudo-NMOS gates dissipate power when the output is low

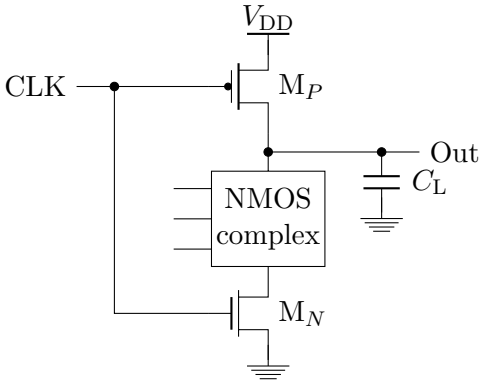


If both A and B are high, then a path exists to Gnd. Otherwise, the output remains high and we preserve the value on the capcitance at the output node. This charge storage at the output node makes it a dynamic gate.

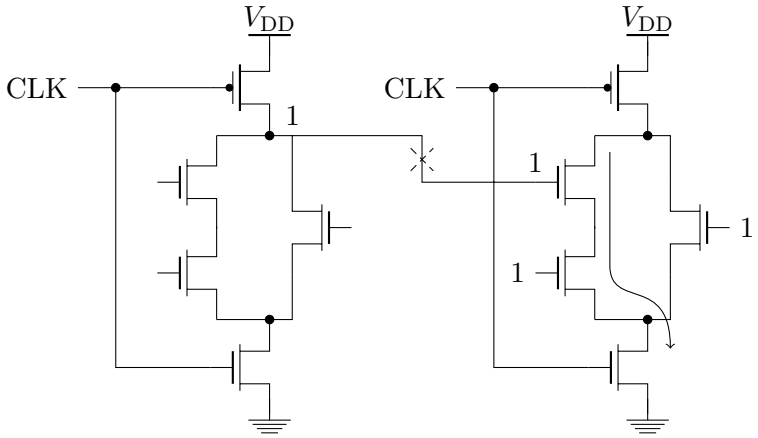
7.4.1 NOR3 in dynamic logic



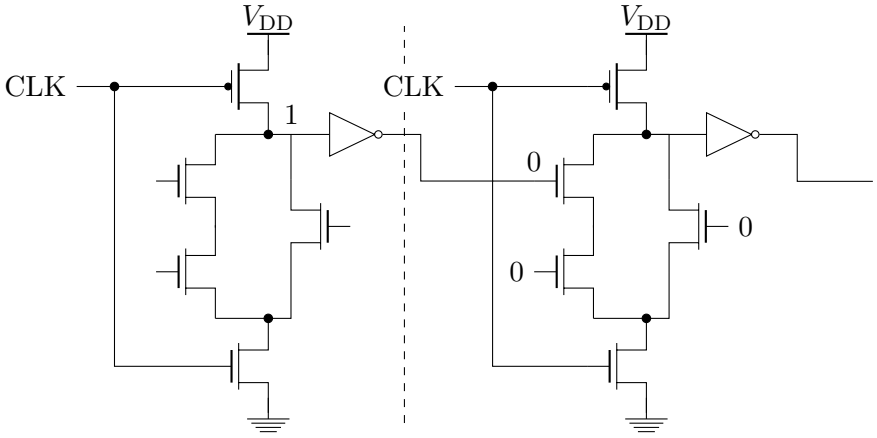
In reality, the CLK signal arrives first so A, B and C can be considered as late arriving signals. In that case, the transistors can be reduced to half the size to deliver the same delay as the inverter.



The desired function is implemented in the NMOS complex. Transistors M_p and M_n are the precharge and evaluate transistors, respectively. The foot transistor is the only extra device relative to pseudo-NMOS gates.
Note that all dynamic gates require a clock signal for proper operation.



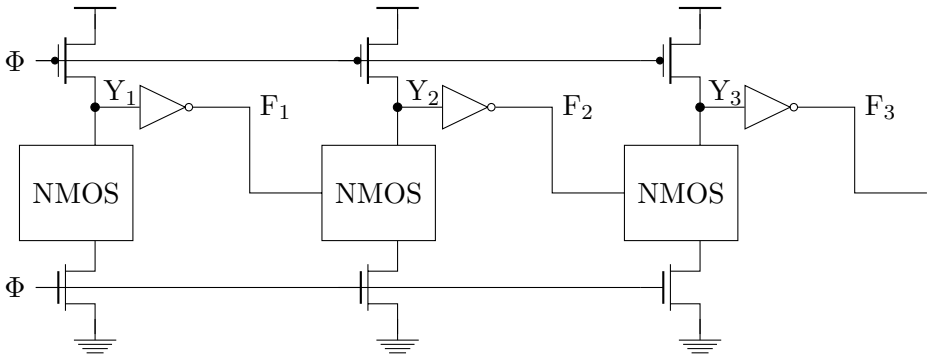
a) Direct connection not possible



b) Insert inverter between dynamic gates

Define a stage as the dynamic gate plus the inverter.
The output pf each stage is now low during precharge. Therefore, all NMOS transistors are off during precharge and can only be turned on during the evaluate phase.

⇒ domino stage (dynamic stage + inverter)
⇒ domino logic circuits



The clock, Φ, should only be low until all inverter outputs are low. When Φ goes high, we enter the evaluation phase where the internal nodes (labeled Y_1, Y_2, Y_3) will fall like dominos in order from left to right, assuming there is a path to Gnd through their respective n-complexes.

The clock must remain high long enough for logic to propagate through the entire chain.

- high duty cycle (percentage of time that the clock is high)
- we care most about the falling edge of the dynamic block and the rising edge of the inverter output

⇒ Stronger pull-down in the dynamic gate
Stronger pull-up in the static inverter

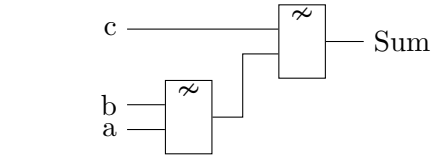
$\Rightarrow$ V_S of inv is higher (skewed)

$\Rightarrow$ V_S of gate is lower ($\approx V_{TN}$)

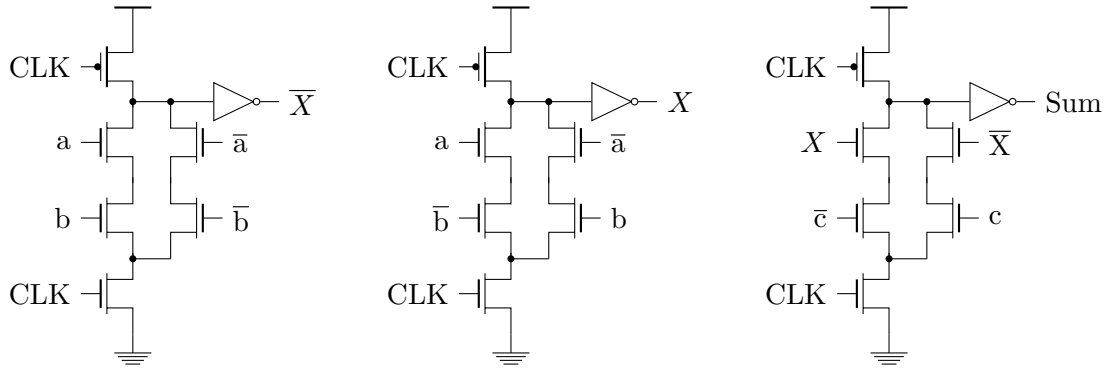
$\Rightarrow$ Therefore, a domino stage will actually switch earlier than a regular gte

There is also a power savings in domino logic. Only those gates that discharge to Gnd will dissipate power. There will be no power dissipation due to crowbar current since a direct path between V_{DD} and Gnd is not allowed in this type of logic. In addition, glitches can be effectively removed since all inputs switch from low to high.
It can onl be used to create noninverting functions.
$\Rightarrow$ An inverter cannot be implemented in domino logic

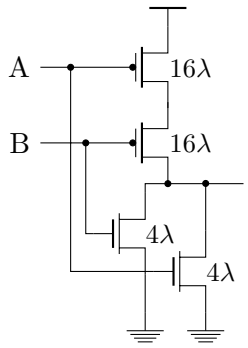
7.4.2 Adder function in Domino Logic



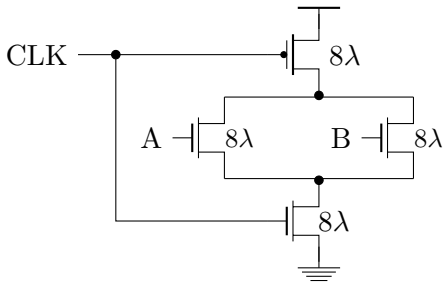
$$X = a \oplus b = a\overline{b} \vee \overline{a}b$$
$$\overline{X} = \overline{a \oplus b} = ab \vee \overline{a}\overline{b}$$
$$\text{Sum} = c \oplus X = c\overline{X} \vee \overline{c}X$$



7.4.3 Logical Effort for Domino Gates



a) static NOR gate



b) dynamic NOR gate

$$\mathrm{LE}_{\mathrm{nor}} = \frac{5}{3}$$
$$\mathrm{LE}_{\mathrm{dyn\_nor}} = \frac{C_{\mathrm{in,gate}}}{C_{\mathrm{in,inv}}} = \frac{8\lambda}{12\lambda} = \frac{2}{3}$$
$$\mathrm{LE}_{\mathrm{inv}} = 1 \Rightarrow \mathrm{LE}_{\mathrm{avg}} = \sqrt{\frac{2}{3} \cdot 1} \approx 0.8$$

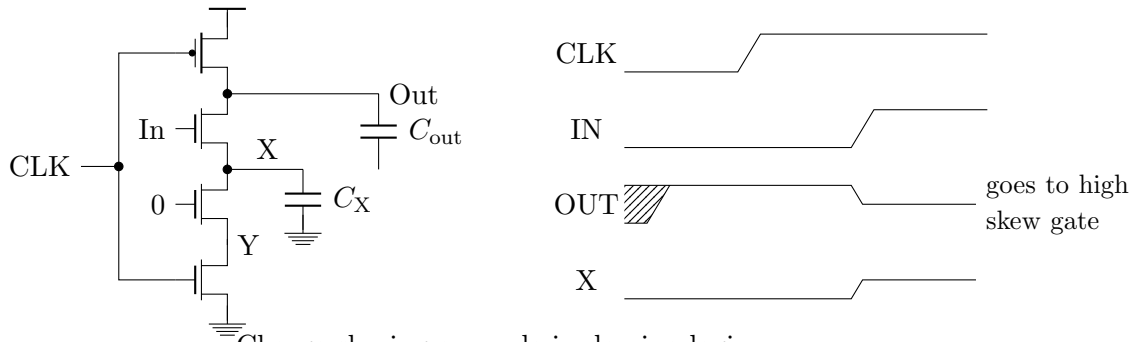
Therefore, the domino stage is better in terms of its overdrive capability and inout capacitive loading.
⇒ Only one NMOS device is driven in the domino case
⇒ PD does not fight with the PU, $V_{\mathrm{S}} \approx V_{\mathrm{TN}}$

7.4.4 Limitations of Domino Logic

There are notable disadvantages that have prevented its widespread use in industry.

- potential for logic upset due to charge loss on a capacitor
- charge sharing (zwei getrennte Kapazitäten zusammenschalten)
- noise injection due to capacitive coupling
- charge leakage
- α-particle hits

Once lost, it cannot be recovered and the circuit ceases to function correctly.



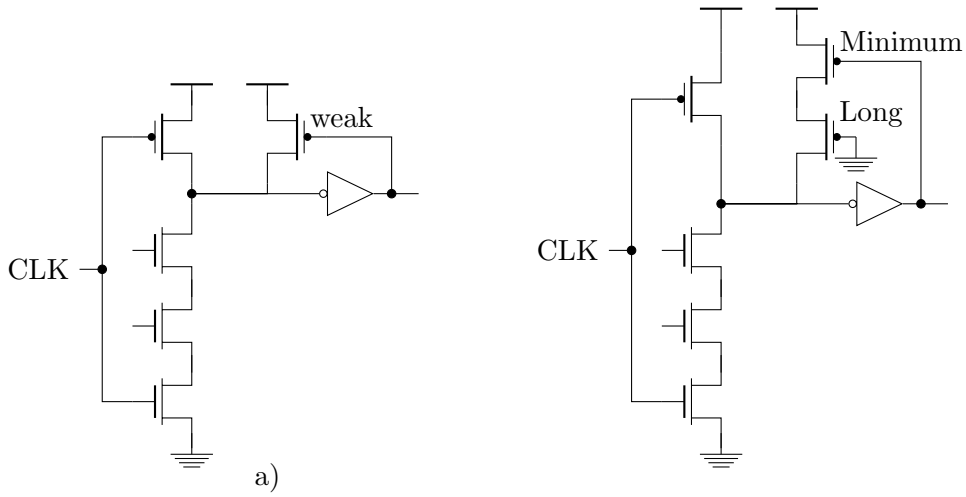
Charge-sharing example in domino logic

The degree of charge sharing depends on the two capacitances C_{out} and C_{x}.

$$V^* = \frac{C_{\mathrm{out}}}{C_{\mathrm{x}} + C_{\mathrm{out}}} V_{\mathrm{DD}}$$

If they are equal, then the output valve will be reduced to half its original value (i.e. $0.5V_{\mathrm{DD}}$).
There is obviously a design tradeoff between timing and noise tolerance when sizing the

inverter.

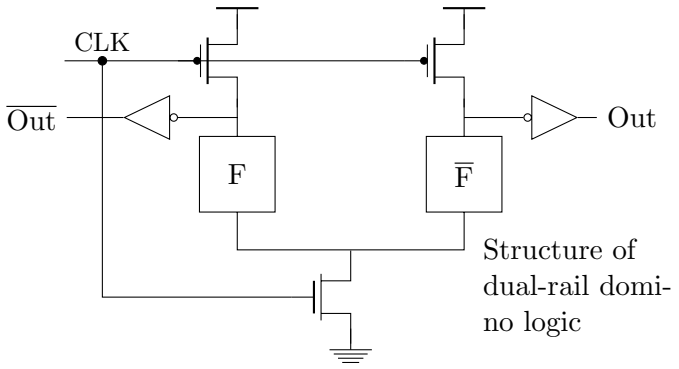


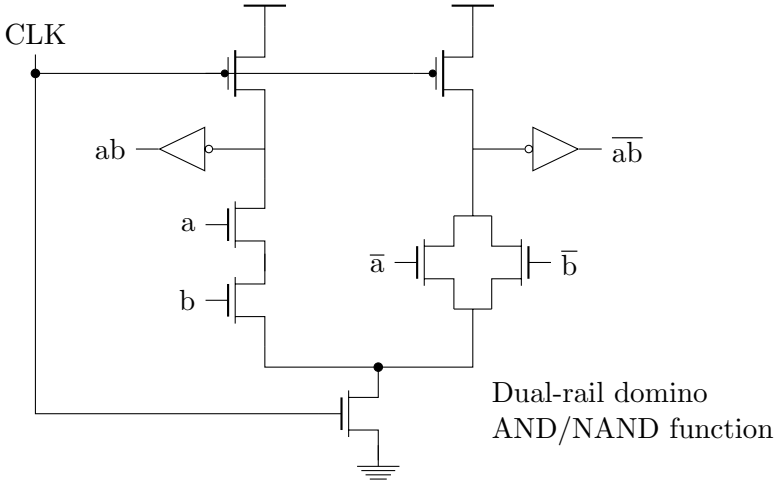
a)

Minimizing the effects of charge sharing using Keepers.
Keepers or baby-sitters: weak PMOS $\Rightarrow \frac{W}{L}$ is small
Discussion: siehe Buch Seite 344-345

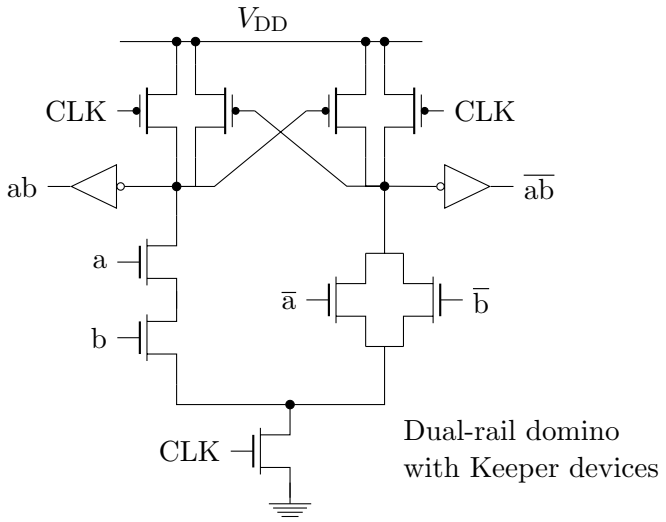
7.4.5 Dual-Rail (Differential) Domino Logic

- Differential Cascode Voltage Switch (DCVS) logic
- complementary pair of logic outputs



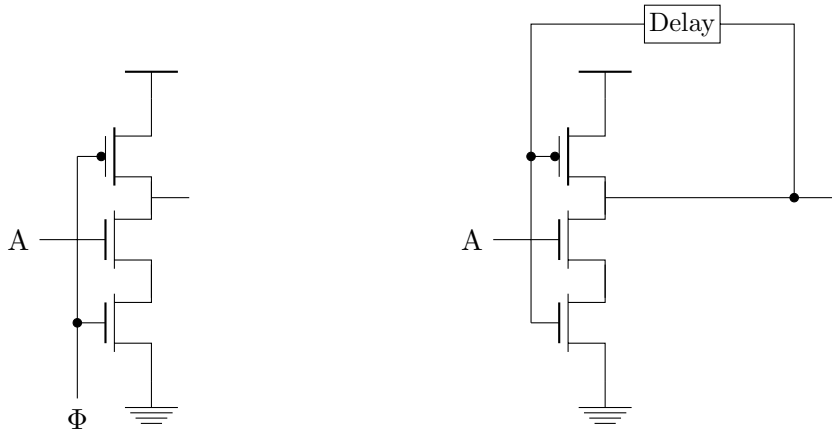


- internal nodes are susceptible (anfällig) to charge sharing
- power dissipated is much higher since one side will always be precharged high and then go low
- but: not every logic gate requires a complement function



7.4.6 Self-Resetting Circuits

Delay and skew from clock to dominio gates
⇒ Automatically precharge (i.e. reset themselves) after a prescribed delay



a) Precharge circuit b) Postcharge circuit

The delay line is implemented as a series of inverters. The width of propagating pulses must be controlled carefully or else there may be contention between NMOS and PMOS devices or, even worse, oscillations may occur.
For example, if A is high for more than twice the delay around the loop, the circuit will oscillate. Therefore, special care must be take to ensure correct timing.

Literatur

[1] David Hodges, Horace Jackson, and Resve Saleh. *Analysis and Design of Digital Integrated Circuits*. McGraw-Hill Science/Engineering/Math, 2003.